March 2011- February 2012

Center for Embedded Systems

An NSF Industry/University Cooperative Research Center

Results Report: Year 3

National Science Foundation

ASU Ira A. Fulton Schools of Engineering
ARIZONA STATE UNIVERSITY

SIU Southern Illinois University CARBONDALE

In This Report:

3rd Year Research Results:

Center for Embedded Systems

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Results Report: Year 3

About The Center for Embedded Systems

The Center for Embedded Systems (CES) is a research collaboration between academia (Arizona State University and Southern Illinois University Carbondale), industry (leading electronics companies throughout the world) and government (the National Science Foundation). Its purpose is to advance the field of embedded systems in algorithms, applications, and architectures to new levels; thereby, sharing resulting technology advancements and commercializing applications to advance commerce.

CES was founded by the National Science Foundation as an industry/university cooperative research center (I/UCRC) in 2009. The center conducts industry-university research projects that are funded by its industry members, the NSF and the two participating universities. CES provides research support for students and faculty, sponsors an internship program, and administers a relevant embedded systems curriculum. Industry members share the intellectual property resulting from all research projects.

This report summarizes research results for the Center's third year of operation as an NSF I/UCRC.

Academic Members:

Ira A. Fulton Schools of Engineering, Arizona State University

Southern Illinois University

Industry Partners:

Intel AZ

Caterpillar

Raytheon

Qualcomm

Intel OR

General Dynamics

EMAC, Inc.

Toyota

Intel CA

DICKEY-john

UTC Aerospace Systems

Marvell

Rockwell Collins

Research Areas of Expertise

Power, Energy and Thermal Aware Design

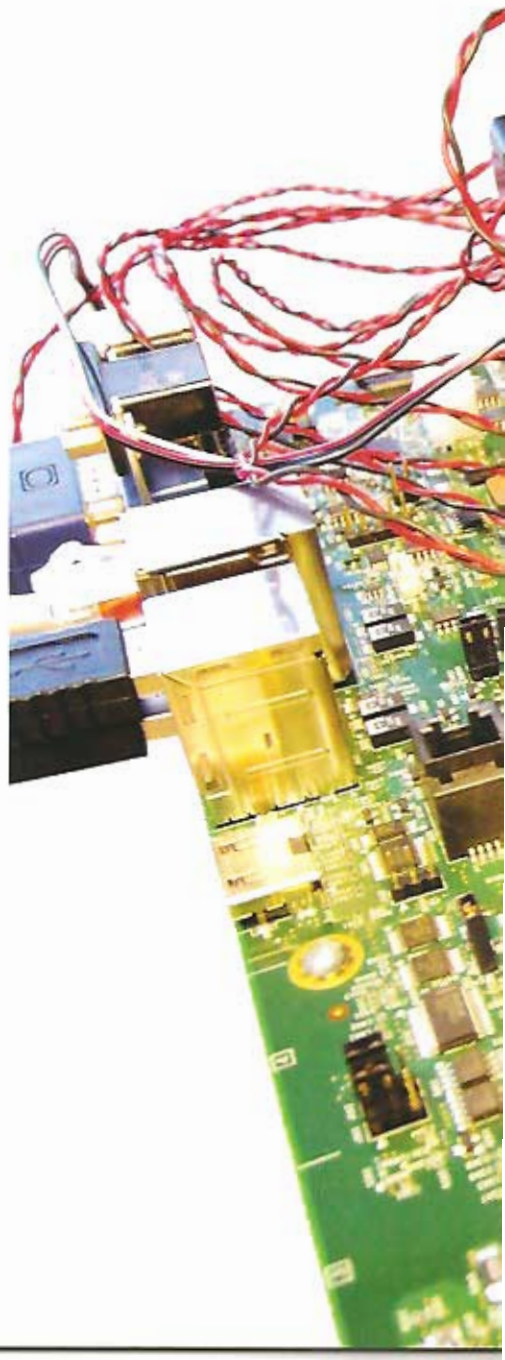
- Low power circuit architectures and design tools
- Dynamic performance, power, energy and thermal management for multicore embedded systems
- Statistical variation aware design of digital systems
- Energy efficient architectures and code optimization for embedded systems

Electronic System-level Design (ESL) and Technologies

- Modeling and simulation
- Hardware/software co-design and optimization
- Trusted, reliable, and secure design

Embedded Multicore Architectures and Programming

- Network-on-Chip design and optimization
- Compilation of stream applications on multicore processors
- Highly power-efficient programmable accelerators
- Soft error resilient system design
- Design and programming of low power embedded systems
- Embedded GPU computing
- Temperature- and variations-aware architectures and programming



Embedded Software System

- Real-time scheduling
- Embedded systems for smart grids
- Middleware and VM for embedded systems
- Embedded software instrumentation and tools

Cyber-Physical Systems

- Modeling and simulation
- Model based formal verification and semi-formal testing
- Model based synthesis from high-level specifications

Integrated Circuit Technologies, Design, and Test

- Semiconductors for hostile environments
- Device physics and modeling
- Microelectronic device and sensor design and manufacturing
- Analog/RF/mixed signal circuit design and test
- Testing and silicon debug of digital circuits

Visit our website for more research information at:

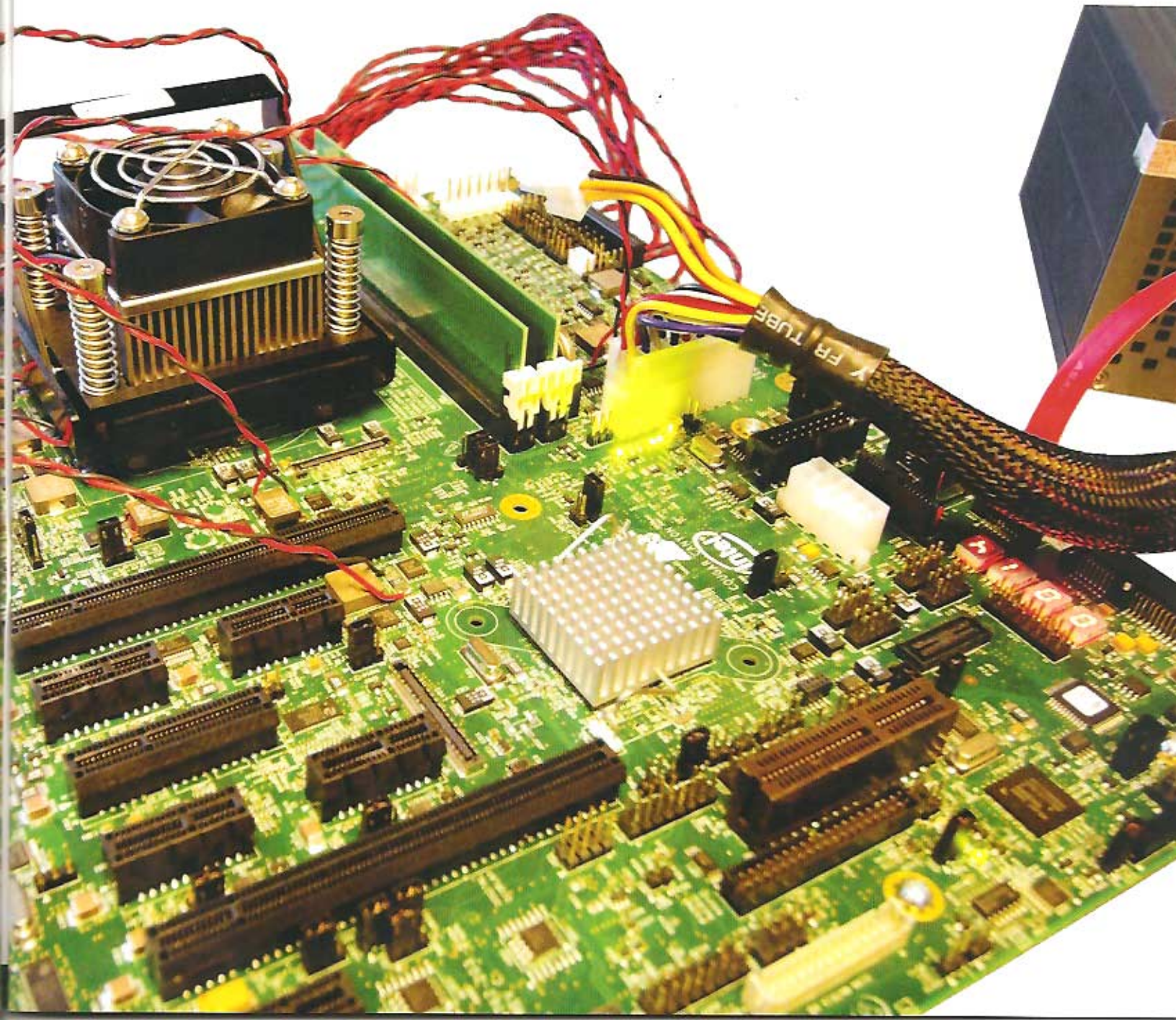
embedded.engineering.asu.edu

Technology Advances and Economic Impact

CES Metrics/Economic Impact

2	Universities
13	Industry Members
16	Research Projects
16	Faculty Researchers
2	Professional (staff)
8	Research Associates (bachelors)
17	Research Associates (masters)
13	Research Associates (doctorates)

24	Industry Internships
11	Graduates
20	Presentations
20	Research Publications
4	Products / Tech Transfer
0	Patents



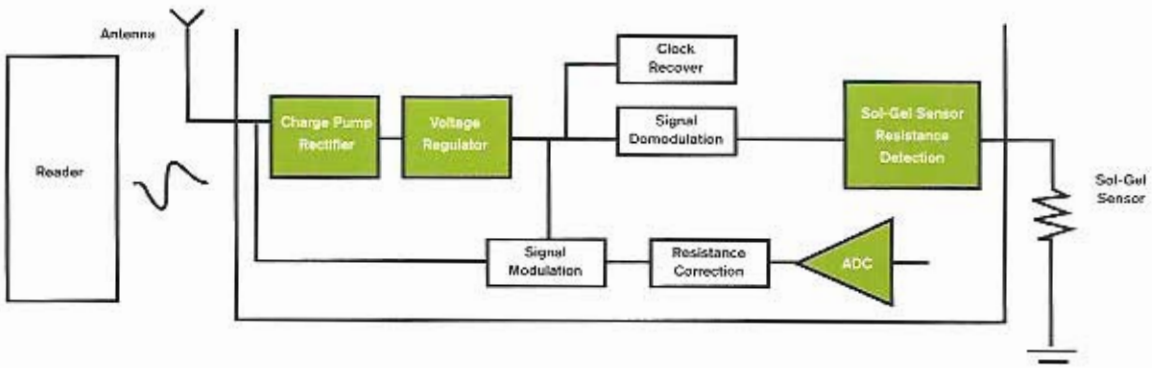
Technology Advance: Monitoring Bridge Conditions Now Easier, Thanks To Low-Power Wireless Sensor Circuits

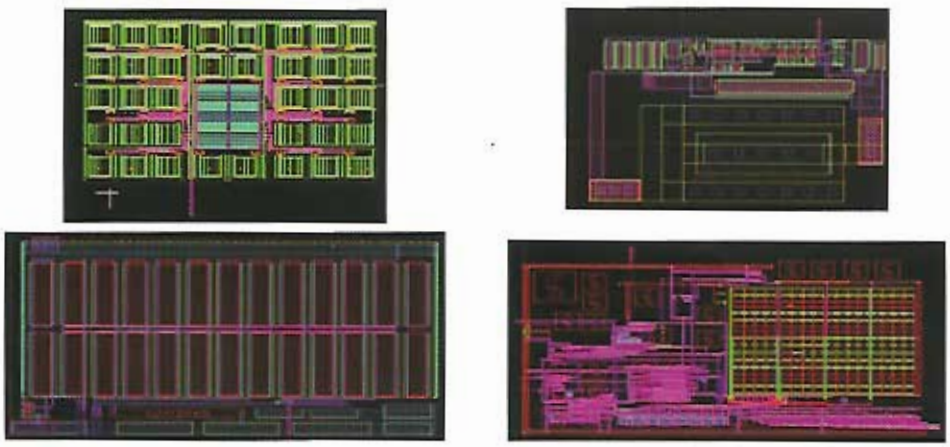
Our national transportation infrastructure includes many bridges that are close to (or exceed) their expected life cycles. The conditions of these bridges need to be closely monitored to ensure the safety of millions of drivers who drive on them each day. Currently, monitoring bridge conditions is a labor-intensive and costly process. Sensor techniques have emerged as promising solutions to achieve more cost-effective and accurate bridge condition monitoring. Specifically, wireless sensors are more desirable because of their low-cost installation procedures.

Currently, most wireless sensors developed for bridge monitoring applications are powered by either batteries or power lines fixed at bridges. The former requires regular maintenance (for replacing depleted batteries) and the latter limits where the sensor devices can be installed. To overcome these limitations, researchers at the Center for Embedded Systems developed circuit techniques for implementing ultra-low power wireless sensors, which can be powered by energy harvested from radio frequency (RF) signals. Therefore, such sensors can be installed at any desirable locations without worrying about the accessibility for future maintenance or the availability of power lines. These circuits are tailored to work with a type of sol-gel sensors that can be used to monitor bridge corrosion.

The developed novel circuits include an efficient energy harvesting circuit, ultra-low power voltage regulator, and low-power analog to digital converter (ADC) circuits, which are major components of the battery-less wireless sensor circuits as shown in the figure below. The circuits are optimized according to the characteristics of the sol-gel sensors. The outcome of this research provides key circuit components to implement the wireless sensor working with sol-gel sensors for bridge monitoring applications. In addition, the developed circuit techniques can be used in wireless sensor design for other applications.

Wireless sensor circuit to work with sol-gel sensors for bridge corrosion detection





Economic Impact:

Using wireless sensors with energy harvesting capability to monitor the conditions of bridges or other civil structures not only improves detection accuracy, but also significantly reduces monitoring cost by reducing the need for field visits. The developed novel low-power circuits are critical components to implement low power sensors for bridge monitoring applications.

Technology Advance: Keeping IP Safer - A JTAG-Based Device Security Architecture for Embedded Systems

The Joint Test Action Group (JTAG) interface has become a powerful interface for embedded components, especially microcontrollers. Common features currently deployed with the interface are reading and writing of memory and the debugging of the system core. The deployment of the interface has allowed for easier access of the system internals making debugging easier. However, the same interface has given adversaries unprecedented access to intellectual property stored on a chip which can be stolen or modified.

Current security mechanisms for the JTAG interface have used static or dynamic keys that require the unlocking of a device. However, once the device is unlocked, all the intellectual property is exposed. This two-level security mechanism requires that there is a high level of trust placed upon those who have the keys. The Center for Embedded Systems has investigated alternative JTAG security schemes which allow for a greater number of user privilege levels. The result is a security hardware architecture that can allow the user to perform system diagnostics with the JTAG interface without compromising the intellectual property.

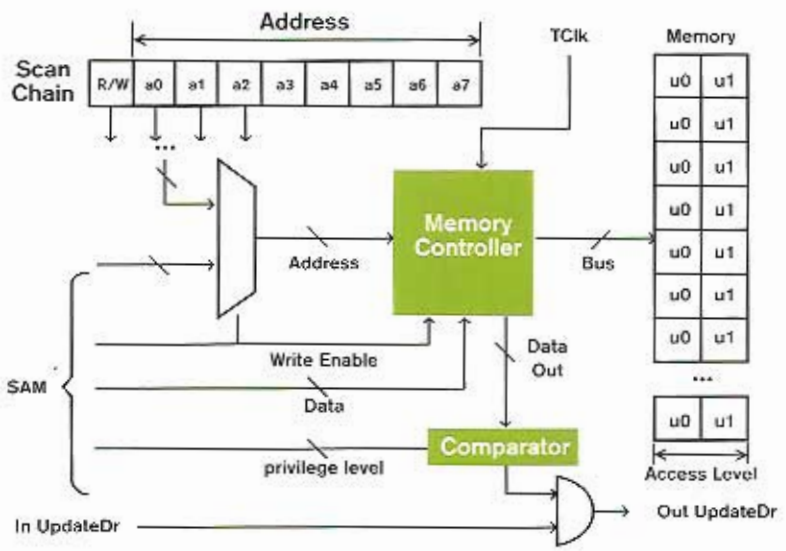
The security architecture works by inspecting every incoming JTAG instruction to see if the authenticated user has the privilege to execute that instruction. The advantage of this is that features of the JTAG interface can be turned on/off depending on the authenticated user. For instance, it is possible to prevent access to the memory where the software is stored, but allow access to the microchip's internal tests. Under this scheme it is even possible to partition the memory into secure and unsecure partitions.

The new JTAG security architecture is compliant with the IEEE 1149.1 standard. Furthermore, the architecture does not introduce additional timing overhead, but instead leverages the JTAG architecture. This allows for easy deployment of the security mechanism in existing designs.

Economic Impact:

The security mechanism provides protection for intellectual property. This helps companies guarantee return on investment for expensive product development. By minimizing risk, companies will have greater incentive to bring innovations to the consumer market.

JTAG Security Architecture for Scan Chains



Center Work Products | Publications

1. Acevedo, O., Kagaris, D., Poluri, K., Ramaprasad, H. and Warner, S. "Towards Optimal Design of Avionics Networking Infrastructures," in *Proceedings of the 31st Digital Avionics Systems Conference (DASC)*, October 2012.
2. Bai, K. and Shrivastava, A., "A software-only scheme for managing heap data on limited local memory (LLM) multi-core processors," ACM TECS: *ACM Transactions on Embedded Computing Systems*, 2012.
3. Bai, K., Lu, D., and Shrivastava, A., "Vector class on limited local memory (LLM) multi-core processors," in *Proceedings of the 14th International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, pp. 215-224, ACM, (New York), NY, 2011.
4. Bai, K., Shrivastava, A., and Kudchadker, S. "Stack data management for limited local memory (LLM) multi-core processors," in *Proceedings of the International Conference on Application Specific Systems, Architectures and Processors (ASAP)*, (Santa Monica, California), September 2011.
5. Dara, C., Tragoudas, S., and Haniotakis, T., "A metric for weight assignment to optimize the performance of MOBILE threshold logic gate," in *Proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology (DFTS 2011)*, pp. 131-138, (Vancouver, BC, Canada), October 2011.
6. Fainekos, G., Sankaranarayanan, S., Ueda, K., and Yazarel, H., "Verification of automotive control applications using S-TaLiRo," in *Proceedings of the American Control Conference*, (Montreal, Canada), June 2012.
7. Gangadhar, S. and Tragoudas, S., "A probabilistic approach to diagnose SETs," in *Proceedings of the 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS 2011)*, pp. 261-267, (Vancouver, BC, Canada), October 2011.
8. Gangadhar, S. and Tragoudas, S., "Accurate calculation of SET probability for hardening," in *Proceedings of the 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2012)*, (Austin, TX), October 2012.
9. Gangadhar, S. and Tragoudas, S., "An analytical method for estimating SET propagation," in *Proceedings of the 29th IEEE VLSI Test Symposium (VTS 2011)*, pp. 197-202, (Dana Point, CA), May 2011.
10. Jayaraman, D. and Tragoudas, S., "Occurrence probability analysis of a path at the architectural level," in *Proceedings of the IEEE International Symposium on the Quality of Electronic Design (ISQED 2011)*, pp. 464-468, (Santa Clara, California), March 2011.
11. Karmarkar, K. and Tragoudas, S., "Error correction encoding for multi-threshold capture mechanism," in *Proceedings of the 17th IEEE International On-Line Test Symposium, (IOLTS 2011)*, pp. 157-162, (Athens, Greece), July 2011.
12. Lee, H., Che, W., and Chatha, K.S., "Dynamic scheduling of stream programs on embedded multi-core architectures," in *Proceedings of International Conference on Hardware-Software Co-design and System Synthesis*, (Tampere, Finland), October 2012.
13. Lu, D. (2012). *STL on limited local memory (LLM) multi-core processors.* (Master's thesis). Retrieved from ProQuest Dissertations and Theses. (Accession Order No. AAT 1508221).
14. Palaniswamy, A.K. and Tragoudas, S., "An efficient heuristic to identify threshold logic functions," in *ACM Journal on Emerging Technologies in Computing (JETC)*, 2012.
15. Palaniswamy, A.K. and Tragoudas, S., "A scalable threshold logic synthesis method using ZBDDs," in *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI'12)*, pp. 307-310, (Salt Lake City, UT), May 2012.
16. Pierce, L. and Tragoudas, S., "Multi-level secure JTAG architecture," in *Proceedings of the 17th IEEE International On-Line Testing Symposium (IOLTS 2011)*, pp. 208-209, (Athens, Greece), July 2011.
17. Pierce, L. and Tragoudas, S., "Enhanced secure architecture for JTAG systems," in *IEEE Transactions on VLSI Systems (TVLSI)*, 2012.
18. Somashekhar, A.M., Gangadhar, S., Tragoudas, S., and Jayabharathi, R., "Non-enumerative generation of statistical path delays for ATPG," in *Proceedings of the International Conference of Computer Design (ICCD 2012)*, (Montreal, Quebec, Canada), September 2012.
19. Watkins, A. and Tragoudas, S., "Transient pulse propagation using the Weibull distribution function," in *Proceedings of the 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2012)*, (Austin, TX), October 2012.
20. Yang, H., Hoxha, B., and Fainekos, G., "Querying parametric temporal logic properties on embedded systems," *International Conference on Testing Software and Systems*, (Aalborg, Denmark), November 2012.

Tools

1. Open source curriculum modules: http://www.engr.siu.edu/~weng/ece424/index.html
2. Software tool: Avionics Network Evaluation, http://heera.engr.siu.edu/ces/files/AvionicsProject.zip
3. Software tool: BDD Software Tracing Tool, http://www.engr.siu.edu/ces/files/GeneralBDDTracer.zip
4. Software tool: External Security Module using openOCD, http://www.engr.siu.edu/ces/files/jtag-openocd.tar.gz

A Light-Weight Runtime Multi-Tasking Scheduler for Embedded Multi-Core Architectures

Researcher: **Karam S. Chatha** | Student: **Haesung Lee**

Project Overview

Problem

Generate an execution schedule for a dynamical changing set of applications on the embedded multi-core architecture

Description

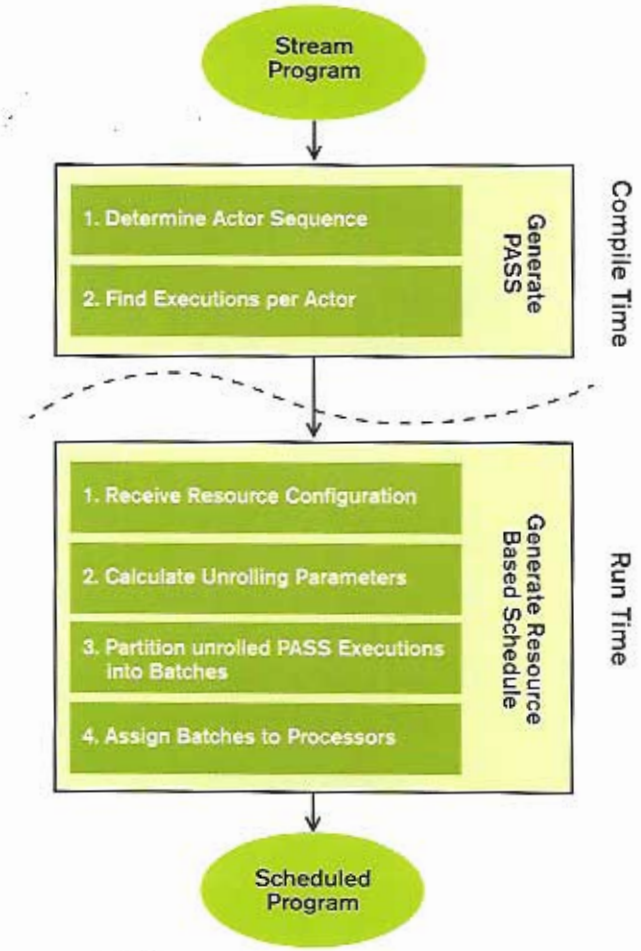
Development of a run-time (dynamic) scheduler for solving the parallel execution problem on embedded processors

Dynamic Scheduler Overview

- Focus on streaming applications
  - Common in high performance embedded applications
  - communication, multimedia, graphics
- Two-step approach
  - Compilation into a flexible resource usage format
  - Dynamic scheduling based on workload requirements

Highlights/Technology Transfer

- Demonstrated by simulations and actual implementation that dynamic scheduling is effective for streaming applications
- Experimental results demonstrated improvements of 5 to 6 times against state-of-art dynamic scheduling approaches
- Showed performance improvement of 3 times against a compilation based approach



Project Tasks Deliverables

Collect use cases and generate stream models	Qtr 1	Completed
Devise the algorithm for run-time scheduling	Qtr 2	Completed
Implement the simulation framework for validation	Qtr 3	Completed
Improve the algorithm and generate final report	Qtr 4	Completed

Development of Fast Grain Quality Measurement System

Researchers: **Ying Ada Chen, Jun Qin**
Students: **Shiyu Xu, Linlin Cong, Leanna Smith**

Project Overview

Problem

This program pursues an optical approach to grain grading, not to replace the official grading method, but rather to provide a fast and effective preliminary screening in locations where the official method is not practical.

Description

This project is to develop a grain quality measurement system that provides a fast, less subjective, and cost-effective grading method, based on optical imaging and computer recognition techniques.

Highlights/Technology Transfer

- The proposed fast grain quality measurement system will open a new market and allow the member company to meet a need in the industry.
- The proposed device would also benefit both farmers and grain handlers in providing quantitative information that is less subjective.

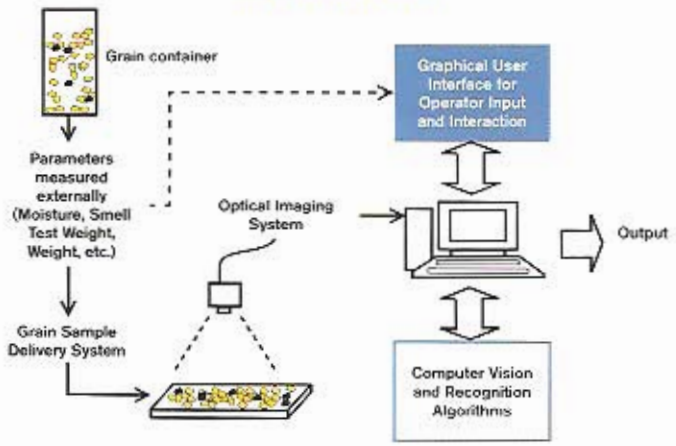
Executive Summary

- To improve optical imaging system, computer recognition algorithms and operator interface.
- To integrate major components together for grain grading purposes.

Phase II Progress (August 2011- August 2012)

- The system and computer vision algorithm were improved.
- The developed system and algorithms were validated based on experiments and statistical analysis to focus on corn grading.

System Diagram



Project Tasks Deliverables

Development of lab bench test system with computer vision algorithms and graphical user interface	December 2011	Completed
Algorithm Outline for review	January 2012	Completed
Design Review of the desk-top prototype system; complete experimentation of base plate, cameras, and lighting	March 2012	Completed
Final construction of Bench-top prototype system	April 2012	Completed
Improve corn grading algorithm with emphasis on statistical correlation	June 2012	Completed
Demonstrate repeatability and reproducibility of the grading system	July 2012	Completed

Enhancing Embedded Systems Curriculum using Atom-based Platform

Researchers: **Ning Weng, Haibo Wang** | Student: **Cheng-Liang Hsieh**

Project Overview

Problem

Address the gap between modern embedded computing and existing embedded system curriculum

- modern embedded systems leveraged with computing power and network connectivity, have evolved significantly and moved aggressively into the industrial, medical, military and home/personal applications
- traditional embedded system curricula are mostly based on microcontroller-based systems and targeted primarily in industrial control applications.

Executive Summary

Curriculum emphasizes on systematic perspective and hands-on experience by leveraging Intel platform and software modules into course labs.

- Enhance the curriculum on embedded systems and applications by leveraging Intel Atom-based platform and software modules
- Develop course modules emphasizes on systematic perspective
- Design hands-on labs to prototype a simplified intelligent heath care gateway
- New project-based learning approach: Class project with pretended industrial setting (clapping).

Highlights / Technology Transfer

Open source curriculum modules:

- http://www.engr.siu.edu/~weng/ecc424/index.html

Course offered

- Independent study course, Spring 2012
- Regular course, Fall 2012
- Course project received an honorable mention in Cornel Cup presented by Intel

Project Tasks Deliverables

Development lecture materials	January 2012	Completed
Understand lab targeting platform architecture and design process	February 2012	Completed
Offer the course as independent study	May 2012	Completed
Develop more lab modules	August 2012	Ongoing
Incorporate materials into a regular course	August 2012	Completed
Open source curriculum modules: http://www.engr.siu.edu/~weng/ece424/index.html	December 2012	Ongoing

Feasibility of Integrating Memristors and Threshold Logic for Compact, Low Power Digital Circuits

Researchers: **Hugh Barnaby, Sarma Vrudhula** | Student: **Debayan Mahalanabis**

Project Overview

- Design CMOS threshold logic circuit consisting of sense amplifier and memristor-based input network.
- Fabricate CMOS circuit and perform post processing to integrate memristors.
- Test functionality and measure performance and power.

Problem

Feasibility of integrating memristors and CMOS threshold logic for compact low power circuits

Highlights/Technology Transfer

Fabrication and verification of CMOS sense amplifier circuitry completed

Characterization of memristor devices has been performed

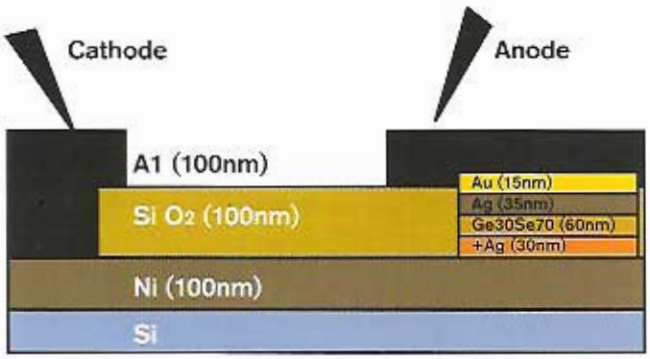
Some processing issues with packaging of memristor devices possibly due to thin nature of device pads

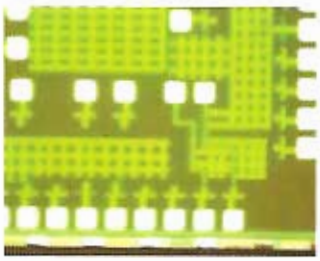
Currently in the process of resolving the issues and fabricating new devices to perform integration with CMOS chip and verify functionality of threshold logic gate

Executive Summary

Goals

- Build a threshold cell library combining threshold cells with memristors to realize hybrid networks
- Expectations: significant reduction in area and power
- CMOS chip (below) to be integrated with memristor devices (cross section shown below)





Project Tasks Deliverables

Develop a behavioral model of the memristor (in VerilogA language) that can be simulated in Cadence environment.	September 2011	Completed
Build a circuit for a threshold logic gate, which consists of a CMOS sense amplifier and an input network of memristors. Perform simulations in Cadence.	December 2011	Completed
Fabricate the CMOS design and verify functionality	April 2011	Completed
Perform characterization of fabricated memristors through DC switching test and AC Impedance measurement.	August 2012	Completed
Perform post-processing to integrate the memristor input network with the CMOS chip.	September 2012	Complete
Perform tests for functionality, power and performance on the integrated chips.	October 2012	Complete

Feasibility Study for Improving Reliability of an MSP430 Embedded System

Researcher: **Spyros Tragoudas** | Student: **Spyros Adam Watkins**

Project Overview

Problem / Rationale

- Flash based microcontrollers may have reliability problems. In a system controlling safety critical functions, loss of flash memory integrity may harm personnel operating the system
- Write cycles cause breakdown of the gate oxide causing dependability problems
- Charge-Trapping Leakage often occurs reducing the reliability for long term data storage after exposure to random or cyclic thermal cycles

Project Description

Improve the reliability of a MSP430 platform such that no single point failure will cause a catastrophic system failure

- Find an embedded logic system with memory elements less susceptible to faults under long term product life requirements.
- The solution must be low power, small, durable, and low cost.

Characteristics of MSP430F2131

- Texas Instruments
- 8 KB Flash Memory
- Up to 16 MHz Frequency
- 256 B SRAM
- Power Consumption
- 2.25mA @ 8MHz
- 72µA @ 100kHz
- 16 GPIO Pins

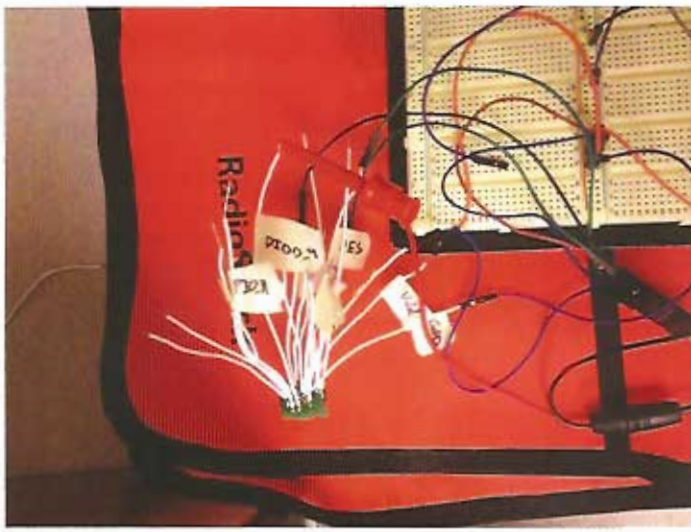
Executive Summary

The system must be designed so that there are no single point failures

- An additional microcontroller must be carefully selected
- The selected microcontroller must be fast, power efficient and small in size

The system must be reliable

- ROM based microcontrollers are more reliable but not available
- Flash memories can be verified using a CRC-16 algorithm and an external check circuit



Project Tasks Deliverables

Feasibility study of suitable microcontrollers	August 2011	Complete
Study Preventing Single-Point Failures	June 2012	70%
Develop and Verify Prototype	August 2012	Complete

Improving Usability of Multicore DSPs with Scratchpad Memories

Researcher: **Aviral Shrivastava** | Student: **Jian Cai**

Project Overview

Project Description

- Irreversible trend of increasing number of cores
- Only distributed memory architectures scale
- Difficult to program distributed memory architectures

Problem / Rationale

- Need explicit data management
- Need explicit communication management

Executive Summary

Objective

- Making it simpler to use multi-core DSPs with SPMs (TI C6678)
- Compiler automatically manages data

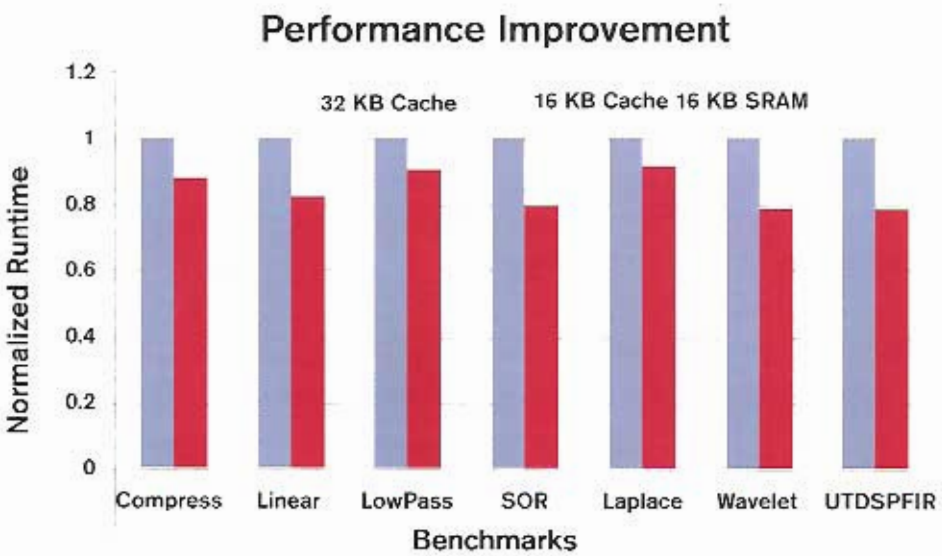
Steps - Source-to-source transformation to do double-buffering of loops

- Find the loops to transform
- Find the required data
- Enable reuse

Done

- Implemented in the CETUS Source-to-source compiler
- Demonstrated the performance benefits of using SPM

Using DMA improves performance by 12%



Project Tasks Deliverables

Setup the 6-core TI-DSP. We can now compile applications for it, run them, and measure performance	Complete
Setup a source-to-source compiler CETUS. Can give a C-code, CETUS compiles it, and re-generates the source code	Complete
Can detect the loops and do the transformation for some very simple loops	Complete

JTAG-Based Device Security for Embedded Systems

Researchers: Spyros Tragoudas, Ning Weng
Students: Joseph Lenox, Luke Pierce

Project Overview

Description

System-level Security Module/Interface for JTAG

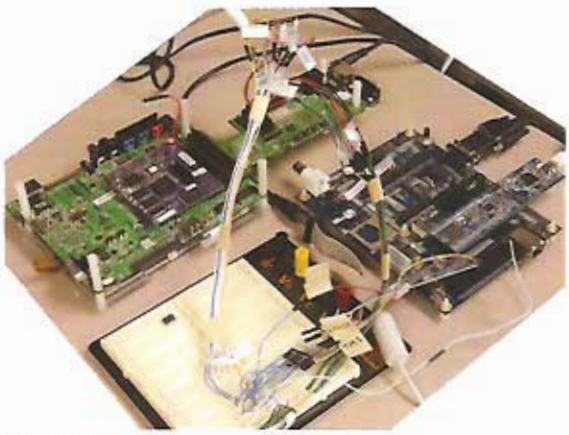
Problem

- JTAG protocol inherently insecure
- Interface usage unmonitored
- Non-standard security

Executive Summary

Permissions-aware JTAG interface

- Restrict unlock key knowledge
- Per-session "key" based on credentials
- Granular access to debug interface functionality



Approach

'Smart' JTAG interface to mediate debug sessions

- Single locked-down MCU
- Dynamic Encryption
- User-level credentials

Re-use existing technologies where practical

- **OpenOCD**
  - Modularized driver interface
  - OpenOCD interfaces to wide variety of debugging solutions, including GDB
- **PHP/Apache/SQL**
  - Standard webserver with scripting fetches user credentials
- **SSL (HTTPS)**
  - Standard key-based cryptosystem for authenticating host systems to server.
- **cURL**
  - Well-used and supported library to perform fetches from HTTPS servers.
- Software prototype tool: External Security Module using openOCD, http://www.engr.siu.edu/ces/files/jtag-openocd.tar.gz

Project Tasks Deliverables

Select Hardware Platform	August 2011	Completed
Complete Hardware Acquisition	August 2011	Completed
Complete Security Module Protocols	February 2012	Completed
Integrate Authentication Module to Back Office	June 2012	70%
Integrate Software Protocols	July 2012	85%
Complete Documentation	July 2012	60%
Demonstrate Prototype	June 2012	Completed

Numerical Modeling of Coupled Thermo-mechanical Processes

Researchers: **Shaikh Ahmed, Jun Qin, Tsuchin Chu**
Students: **Mathew Lane, Bradley Wrage, Caleb McGee**

Project Overview

Problem

Premature failure (e.g. bearing failure) in a high-speed turbine

Project Description

Numerical models for thermo-induced failure in a bearing and heat generation in the entire system need to be created. The model for the bearing should simulate the temperature distribution in a bearing and the critical temperature contributing to bearing failure. Computational fluid dynamic (CFD) analysis should be carried out in order to see how the oil is moving through the system and to quantitate the cooling effects of the oil.

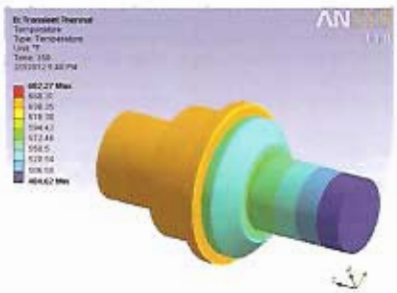
Executive Summary

Thermal Modeling of the system

- Determined the heat flow that is produced by the mating ring seal interface
- Determined the convection coefficient that the system needs to produce in order to see the temperatures that were present in real world testing

CFD Analysis

- Visualize where the oil is flowing within the system
- Couple fluid and thermal models



Highlights/Technology Transfer

- Based on the simulations, the oil-air mixture within the chamber needs to provide an high convection coefficient of at least 800 W/m2 °C in order to keep the bearing temperature at ~600°F, at which the bearing material still loses hardness and lubrications may degrade.

- While the CFD simulations show oil flow out of the outlets used to simulate the bearing, flow interruption that the rotating bearings would cause was not included. A small amount of oil may still be reaching the bearings, however it is most likely not enough to ensure proper operation.

Project Tasks Deliverables

Literature Review	September 2011	Complete
Preliminary Study	October 2011	Complete
Construction of the bearing model	February 2012	Complete
Construction of the system model	February 2012	Complete
Obtain results from both models	February 2012	Complete
Create simple CFD model for validation	May 2012	Complete
Apply conditions to more complex model	June 2012	Complete
Final Report/Deliverables	July 2012	Complete

Platform for Automated Test and Programming of Embedded System on Module

Researcher: **Spyros Tragoudas, Haibo Wang** | Student: **Michael Welling**

Project Overview

Design a carrier complex capable structural boundary scan and functional test of up to 4 modules simultaneously.

Develop structural interconnect testing software that minimizes the overall testing time using structural dependencies and pattern overlapping.

Problem

To effectively parallelize the testing and programming of System on Module (SOM) designs.

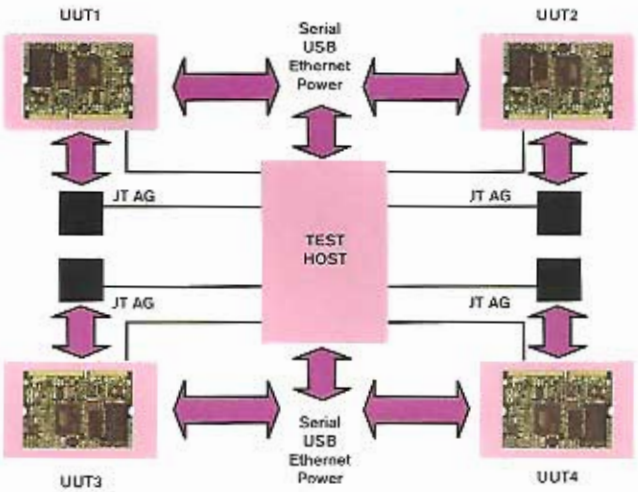
Approach

Design four SOM carrier complex with required interfaces.

- Requested SOM DFT enhancements. (Boundary Scan, Test points)
- PCB manufacturing.
- Hardware / Software integration.

Executive Summary

- **Design a carrier complex capable structural boundary scan and functional test of up to 4 modules simultaneously.**



- **Developing structural interconnect testing software which minimizes the overall testing time using structural dependencies and pattern overlapping.**

Project Tasks Deliverables

Interconnect test pattern generation software.	February 2012	95% Complete
Test pattern application and signature analysis	July 2012	15% Complete
SoM testing carrier schematic capture.	July 2012	6% Complete
Functional test and programming scheme.	August 2012	Re-assigned
Next generation SoM specification.	August 2012	50% Complete
SoM testing carrier PCB layout.	August 2012	On hold

Statistical Fault Grading and Diagnosis

Researcher: **Spyros Tragoudas** | Students: **Ahish Mysore, Ashok Palaniswamy**

Project Overview & Description

Problem

Computing statistical delay and path criticality. Identification of critical paths in the context of process variations.

Project Description

- Main focus of this project is statistical fault grading and diagnosis in the context of process variations
- Path delay fault testing introduces significant challenges in deep-submicron devices
- Delays are modeled using probability density functions (pdfs)
- Probability of each path being critical has to be reported
- Identifying path criticality is an important task and has different applications during the product design cycle
- Exponential number of paths calls for implicit, non-enumerative techniques

Preliminaries – Critical Paths

- Critical paths are those that determine the max delay of a circuit
- They are the longest paths in terms of delay, not necessarily of node counting
- Critical paths are identified by calculating the slack (s) at each node
- slack = Required Arrival Time – Arrival Time (s=RAT-AT)
  - s>0 => AT can be increased without affecting total circuit timing
  - s<0 => Current path is too slow. Apply path optimization
  - s=0 => Path is critical. It determines total circuit delay

Calculating criticality for each path

- **Allows ranking paths according to their criticality**
- **Applications in delay optimization**
  - Optimize only a small set of critical paths
  - Global circuit timing is improved
- **Applications in delay testing**
  - When limited time for delay testing
  - All highly ranked path should be tested

Project Tasks Deliverables

Procedure to consider re-convergences during statistical timing analysis	June 2011	Complete
Statistical path delays using Monte Carlo simulations on ZBDD	January 2012	Complete
Evaluate using Traditional Monte Carlo simulations on netlist	January 2012	Complete
Report the probability of a path being critical for delay defect testing	June 2012	Complete
Path ranking based on the criticality	August 2012	Complete

Statistical Techniques for Property Exploration of Cyber-Physical Systems

Researcher: **Georgios Fainekos**
Students: **Shashank Srinivas, Shih-Kai Su, Subrat Swain, Hengyi Yang**

Project Overview

Problem

- This project studies the problem of automatically discovering the properties that a complex cyber-physical system satisfies .

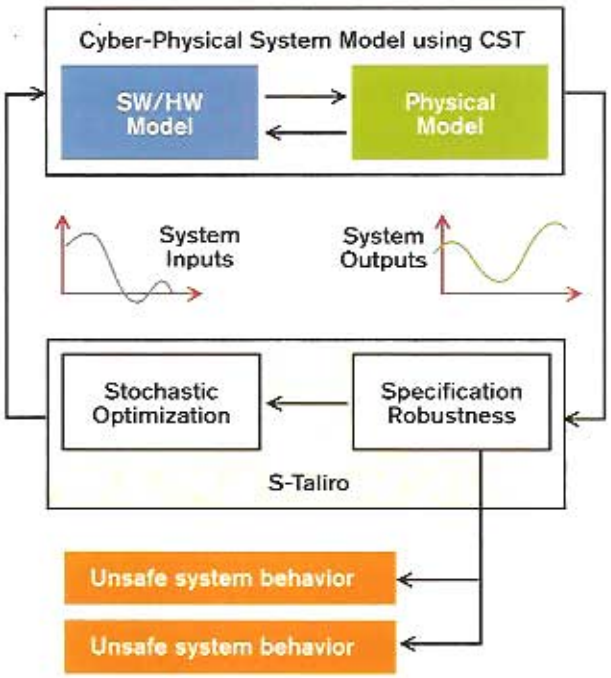
Project Description

- The goal of the project is the development of randomized algorithms and software tools that will return to the user temporal logic formulas that are satisfied on the system under development with guarantees on their satisfaction.

Executive Summary

- The verification of the functional correctness of safety critica cyber-physical systems is a challenging and extremely urger problem

- We developed software tools that will help the designers understand and discover the properties that their systems satisfy



Highlights/Technology Transfer

- Development of new algorithms and software tools for temporal logic robustness computation based on dynamic programming principles

- Development of optimization problems for determining parameter ranges for parametric temporal logic specifications

- The research was conducted in collaboration with the CES industry partner Toyota Technical Center

Project Tasks Deliverables

Implementation of new algorithms for temporal logic robustness computation based on dynamic programming principles.	Quarter 1	Complete
Theoretical results on the problem of estimating parametric real-time temporal logic specifications over general CPS models.	Quarter 2	Complete
Implementation of the theoretical results in the toolbox S-Taliro.	Quarter 3	Complete

Survey and Assessment of Advanced Haptic Technology

Researcher: **Jun Qin** | Students: **Adam Schlag, Ali Mahdi**

Project Overview & Description

Problem

Technical survey of existing haptic technologies in selected application fields: teleoperation, vehicle control, and flight simulation. Detailed investigation of haptic systems in hydraulic control field

Project Description

The project is to provide an assessment of existing haptic technologies in selected fields, and to investigate achievable methods for integration of haptic technology, which is suitable for on-road and off-road operations.

Highlights/Technology Transfer

- The project provided a comprehensive assessment of existing haptic technologies in selected applications fields to the member company, and created a databases of recent publications to member company.
- A detailed comparison of existing haptic technologies in hydraulic control fields has been investigated.
- Potential suppliers of haptic technologies were indentified, and helped member company investigate a low-cost method for integration of haptic technology.

Project Tasks Deliverables

Survey of existing haptic technologies in selected fields: teleoperation, vehicle control, and flight simulation	December 2011	Completed
Provide a database of recent publications which are directly related to haptic technologies in each selected fields	December 2011	Completed
A detailed comparison of existing haptic technologies in hydraulic control field	May 2012	Completed
Identify potential suppliers for providing haptic technology	August 2012	Completed
Final report, documentation, and presentation of findings	August 2012	Completed

Towards Optimal Design of Networking Infrastructure in Avionics Networks

Researchers: Dimitri Kagaris, Harini Ramaprasad
Students: Oscar Acevedo, Kaushik Poluri

Project Overview & Description

Project Description

To transform the process of making design decisions for avionics networking infrastructures from an ad-hoc, empirical approach to a systematic, structured one.

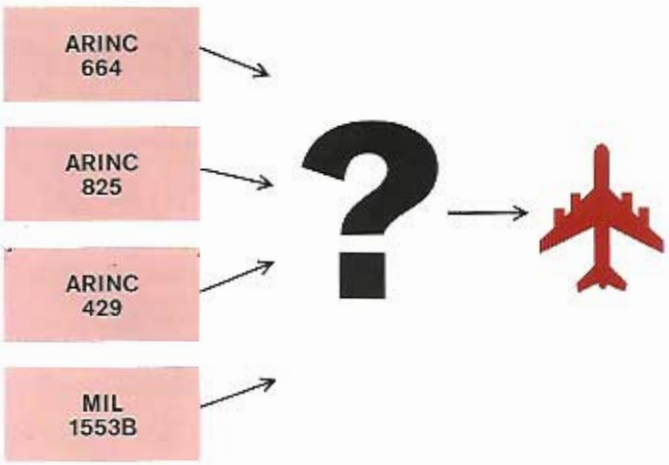
Problem

To develop a tool kit which, given a set of data communication needs

- Shows how a variety of candidate data bus topologies and protocols would perform
- Suggests suitable configuration(s) for the target platform

Executive Summary

- Avionics network infrastructure design is an ad-hoc, empirical approach
- This project presents a systematic, structured approach



Highlights/Technology Transfer

- Comprenhensive report on communication bus technologies
- Software prototype tool: Avionics Network Evaluation, http://heera.engr.siu.edu/ces/files/AvionicsProject.zip
  - Identifies the strengths and limitations of design alternatives
  - Characterizes the behavior of these alternatives
  - Provides guidelines for optimal design to meet the given requirements
- A documented decision tree enabling the user to evaluate and choose appropriate bus architectures and protocol (AHP)

Project Tasks Deliverables

Comprehensive Literature Survey on Communication Bus Technologies	Q1	Completed
Development of Subsystem Decomposition Techniques	Q1	Completed
Development of Subsystem Analysis and System Re-composition Techniques	Q2	Completed
Design and Implementation of Software Prototype for ARINC664	Q2	Completed
Design And Implementation of Software Prototype for MIL-STD-1553B	Q2	Completed
Design And Implementation of Software Prototype for ARINC825	Q3	Completed
Design And Implementation of Software Prototype for ARINC429	Q3	Completed
Decision Tree Process	Q4	Completed
Writing of Comprehensive Project Report	Q4	Completed

Visualization of Software Paths for Efficient Debugging

Researcher: **Spyros Tragoudas** | Student: **Luke Pierce**

Project Overview & Description

Project Description

- Current methods of debugging show only a snapshot of a given point in the code
- Rarely does the snapshot show the point in time where the error occurs, rather gives an indication that an error has occurred.
- To follow how an error occurs many breakpoints are used to recreate the execution history
- For a given breakpoint the historical execution of paths shall be shown giving an indication of where the software error occurs reducing the amount of time needed to find errors
- Storage of the execution paths must be done efficiently for application in multi-core environments

Executive Summary

- Storing of paths in BDDs
  - Using BDDs the executed paths are stored
- Visualization of paths
  - Using JUNG the BDDs are extracted and visualized as directed graphs.

Highlights/Technology Transfer

- GUI Path Execution
- Works for Multi-Core Environment
- Software Source
- Documentation of features and use
- Software tool will plug-in into the Eclipse IDE
- BDD Software Tracing Tool, http://www.engr.siu.edu/ces/files/GeneralBDDTracer.zip

Project Tasks Deliverables

Software Code Labeling	May 2012	Completed
BDD Storage of Executable Paths	June 2012	Completed
Visualization of Executable Paths	July 2012	In Progress
Integration into Eclipse Environment	July 2012	In Progress
Final Prototype Transfer	August 2012	

Center for Embedded Systems

An NSF Industry/University Cooperative Research Center

Results Report: Year 3

> "The Center for Embedded Systems allows Caterpillar to explore research topics which have general benefits for all members, while supporting the particular needs of the company. We also benefit from the research performed for other member companies, as they conduct their respective projects and share results with all members. This is a growing consortium that has not yet realized its full potential."

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