| I/UCRC Executive Summary - Project Synopsis | | Date: 4/14/2016 |
|---|---|---|
| **Project Title:** Accurate and scalable RTL-level fault injection simulation for industrial and automotive standards | | |
| **Center/Site**: NSF I/UCRC for Embedded Systems, SIUC site | | |
| **Principle Investigators: Spyros Tragoudas, Themistoklis Haniotakis** | | **Type: New** |
| **Tracking No**.: | **Phone :** (618 )453 - 7027 | **E-mail :** spyros@engr.siu.edu, haniotak@siu.edu |
| | | **Proposed Budget**: $50,000 |

**Abstract**: Traditional fault injection-based gate-level simulation is non-scalable at the SoC level but industrial and automotive standards require gate-level fault diagnostic coverage. Existing fault simulators that accelerate gate-level fault simulation by considering RTL modules do not meet fault diagnostic coverage standards for industrial and automotive applications. A scalable metric-based fault simulator is proposed. A framework will be developed to evaluate whether the proposed metric-based module-level simulation achieves accurate fault diagnostic coverage. Experimental evidence will be provided. Classes of circuits that require gate-level simulation in order to achieve accurate fault diagnostic coverage will be investigated.

**Problem**: Fault injection-based techniques depend on gate-level simulation but are not scalable due to the size of existing systems on a chip (SoC). At the same time, industrial and automotive standards require that the fault diagnostic coverage be reported at the gate-level. Existing fault simulators that accelerate gate-level fault simulation by considering RTL modules do not meet fault diagnostic coverage standards for industrial and automotive applications. This effort proposes a scalable RTL-level simulator that provides accurate fault diagnostic coverage. Each RTL module may have drastically different netlist representations, and the test set may have drastically different fault diagnostic coverage for alternative netlist representations. The RTL-level simulator should consider an appropriately defined abstract quantity (metric) for each RTL module to derive the fault diagnostic coverage much faster. Appropriate statistical evaluation must be performed to ensure that the approach performs accurately for any test set at any RTL instance. A separate but related problem is to investigate whether there exist RTL-module implementations (netlists) that adopt effective metrics for RTL-level simulation and subsequent conversion to fault diagnostic coverage.

**Rationale / Approach**: In order for the fault simulator to be scalable it should avoid explicit fault simulation. It is proposed to consider an abstract quantity (metric) for each RTL module which provides sufficient information for the underlying netlist so that accurate fault diagnostic coverage estimation is obtained. The values obtained after all patterns are simulated are then translated to gate-level fault diagnostic coverage. Existing RTL-level simulators are either non scalable or consider metrics that do not provide fault diagnostic coverage. The proposal carefully reviews existing approaches and analyzes their weaknesses. The proposed solution relies on a metric quantity that abstracts each RTL netlist while considering the test set. Thorough statistical evaluation will be performed to ensure that the estimated fault diagnostic coverage is accurate and meets industrial and automotive standards. The framework will then be applied to different netlists in order to determine whether certain netlist properties ensure more accurate fault diagnostic coverage. The approach will be evaluated on existing benchmarks available to the academia as well as benchmarks provided to the investigators by the sponsor member company.

**Novelty**:

(a) A new metric quantity for the problem under investigation.
(b) The statistical evaluation framework for the proposed metric.

**Potential Member Company Benefits:**

1. A fast and accurate grading tool to estimate the quality of a given test set in order to assess whether automotive and industrial standards have been met.
2. Thorough experimental evaluation on industrial benchmarks provided by the sponsor company.

**Deliverables for the proposed year:**

1. Software tool to perform RTL-fault grading.
2. Detailed experimental evidence on benchmarks provided by the sponsor company.
3. Determine whether there exist netlist properties that support RTL metric-based accurate simulation.
4. Detailed report and documentation.

| **Estimated Start Date**: 08/16/2016 | **Estimated Knowledge Transfer Date**: 8/16/2017 |
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**Center for Embedded Systems (CES)**
**Request for Proposals Template – YEAR 7**

**DUE:**

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|---|---|---|---|---|---|
| **TITLE:** | Accurate and scalable RTL-level fault injection simulation for industrial and automotive standards | | | | |
| **PIs:** | Spyros Tragoudas<br>Themistoklis Haniotakis | **EMAIL:** | spyros@siu.edu<br>haniotak@siu.edu | **TEL:** | 618-453-7027 |
| **DEPT:** | ECE | **SCHOOL:** | SIUC | | |


**ABSTRACT: (250 OR FEWER WORDS)**

Traditional fault injection-based gate-level simulation is non-scalable at the SoC level but industrial and automotive standards require gate-level fault diagnostic coverage. Existing fault simulators that accelerate gate-level fault simulation by considering RTL modules do not meet fault diagnostic coverage standards for industrial and automotive applications. A scalable metric-based fault simulator is proposed. A framework will be developed to evaluate whether the proposed metric-based module-level simulation achieves accurate fault diagnostic coverage. Experimental evidence will be provided. Classes of circuits that require gate-level simulation in order to achieve accurate fault diagnostic coverage will be investigated.


**PROBLEM:**

Fault injection-based techniques depend on gate-level simulation but are not scalable due to the size of existing systems on a chip (SoC). At the same time, industrial and automotive standards require that the fault diagnostic coverage be reported at the gate-level. Existing fault simulators that accelerate gate-level fault simulation by considering RTL modules do not meet fault diagnostic coverage standards for industrial and automotive applications. This effort proposes a scalable RTL-level simulator that provides accurate fault diagnostic coverage. Each RTL module may have drastically different netlist representations, and the test set may have drastically different fault diagnostic coverage for alternative netlist representations. The RTL-level simulator should consider an appropriately defined abstract quantity (metric) for each RTL module to derive the fault diagnostic coverage much faster. Appropriate statistical evaluation must be performed to ensure that the approach performs accurately for any test set at any RTL instance. A separate but related problem is to investigate whether there exist RTL-module implementations (netlists) that adopt effective metrics for RTL-level simulation and subsequent conversion to fault diagnostic coverage.

**RATIONALE:**

In order for the fault simulator to be scalable it should avoid explicit fault simulation. Methods have been proposed which consider abstract quantities (metrics) for each RTL module. When patterns are applied, a value is computed using the metric which are then translated to gate-level fault diagnostic coverage. The following reviews five recent fault grading methods that accelerate fault grading using this idea, and it is shown that they are not very effective.

The approach in [1] accelerates fault simulation by not considering the netlist of each RTL module. It considers different bit combinations at the inputs of each module M when simulating the test set T. For each bit combination, it also considers the number of times it has occurred. Then a complex formula is used to convert differ bit combinations and their hit count to a hit coverage metric by the test set T. The conversion formula considers the rate that each combination occurs.

Since the approach in [1] does not consider faults, the impact of the hit coverage metric is evaluated by correlating the estimated hit coverage value $x_i$ by each pattern $i$ in T to the actual fault diagnostic coverage $y_i$ by the pattern using the formula below, where N denotes the test set size.

$$\gamma = \frac{N\sum_i x_i y_i - \sum_i x_i \sum_i y_i}{\sqrt{(N\sum_i {x_i}^2 - (\sum_i x_i)^2)(N\sum_i {y_i}^2 - (\sum_i y_i)^2)}}$$

The correlation is shown to be in the range [40% - 70%] for different patterns. The correlation for the test set T is then computed by taking the average value among all patterns. Although the correlation for the test set was high, it was derived by correlating individual patterns, and may not be indicative for the fault diagnostic coverage by the test set T. Therefore the statistical analysis in [1] may not be accurate for safety analysis in the proposed application areas.

Advantages in the approach of [1] is that it scales very well and the simulator takes into consideration clocking and module enabling settings at the modules of the RTL description. However, the metric-based fault estimation is ad-hoc and the experimental results in [1] often show significant difference between the estimated to the actual fault diagnostic coverage. Since the statistical correlation between the estimated and actual fault diagnostic coverage in [1] is not applicable to the examined problems, the approach does not serve well for safety analysis in industrial and automotive applications.

Another metric-based approach is proposed in [2, 3] for a similar problem: Identifying the pattern in the test sequence T beyond which fault diagnostic coverage increases very slowly. This is called the saturation point of the fault diagnostic coverage and the goal is to estimate the fault diagnostic coverage at the saturation point [2, 3]. Their proposed metric becomes insensitive after the saturation point whereas actual fault diagnostic coverage may increase further. Therefore this approach is not well suited for safety analysis in industrial and automotive applications where the fault diagnostic coverage must be computed accurately. Listed experimental results in [2, 3] indicate that the fault diagnostic coverage at the saturation point is either underestimated or overestimated, and this is an additional drawback when trying to achieve a high safety integrity level in the investigated application area.

While simulating the test set T, [2, 3] compute the frequency of different gate input combinations (gic) at each gate. Then the number of different unique combinations at the gates is correlated to the number of faults detected by T. The approach in [2, 3] is not as fast as [1] since it considers the actual netlist of each module M. It is, however, scalable because it performs fault simulation only for a test set of small size. This serves as a mechanism to map the quickly computed metric values to estimated fault diagnostic coverage values when the large test set T is applied. The framework in [2, 3] correlates the gic number sequence to the detected fault diagnostic coverage sequence using linear regression. This statistical methodology serves as the basis for correlating our proposed metric values to fault diagnostic coverage.

The approach in [4] proposes a fault estimation metric using SCOAP controllability and observability values, and correlates more intuitively to testability related problems. The observability and controllability values at each line in a module are used to generate a detection probability for the two faults at the line. Each fault is determined to be either detected or not detected using a threshold value. An inherent drawback of the metric in [4] is that it does not take into consideration the test set T. Since their metric quantity seems to provide the same indication for different test sets, the approach does not relate intuitively to fault diagnostic coverage. In addition, the SCOAP observability metric in [4] only applies to individual modules and not the whole RTL system.

The approach in [4] considers single stuck-at as well as transition fault-coverage. Experimental results in [4] consider industrial benchmarks, and are difficult to replicate. Listed experimental results often show that the estimated fault diagnostic coverage may either underestimate or overestimate the actual fault diagnostic coverage. Furthermore, no statistical evaluation framework is presented in [4].

The approach in [5] relies on systematic fault injection and simulation at the module level. Fault dictionaries are generated for each RTL module M by applying the sequence of patterns at M. Information in fault dictionaries is used to generate the activation probability for each fault and also an estimate of the probability of propagating each fault through the modules in the RTL description. The detection of each fault is determined using the product of these probabilities.

The approach in [5] does not scale well since it requires fault simulation at each module M. Furthermore, there is no statistical evaluation on the fault propagation probability estimate, and the experimental results show that the approach either underestimates or overestimates the actual fault diagnostic coverage. Thus, it is not a promising approach for the investigated problem.

## APPROACH:

Scalability drawbacks of [5] suggest that an acceptable method should rely on a metric quantity that avoids fault injection and fault simulation. The metric should relate more intuitively to fault diagnostic coverage than [1, 2, 3]. The SCOAP-based metric in [4] considered testability measures and inspired our approach. However, in order to serve well for fault grading, the proposed metric should be more elaborate than the one in [4] and also depend on the test set T.

Our metric will not use SCOAP controllability values. When simulating test set T, for each line at any module we will compute the number of times each of the two faults is excited. Each number will then be translated to an activation probability by test set T. That way, a sequence of activation probabilities for each fault will be generated. Fault activation probabilities will be used instead of SCOAP controllability-based probabilities.

Next, we will modify appropriately the well-known method in [6] that computes *sequential* SCOAP observability values for each line. However, instead of using *sequential* SCOAP controllability values we will use the fault activation values that were computed when simulating test set T. That way, the fault observability values will also depend on the test set T. Subsequently, each observability value will be translated to a fault propagation probability. Finally, a sequence of fault propagation probabilities will be generated for each line.

That way, two number sequences will be generated for each fault in the RTL description. Each sequence will have length |T|. The product of each fault activation probability to the respective fault propagation probability will serve as the estimated detection probability for the fault. A sequence of |T| estimated detection probabilities will be generated for each fault. Then a fault estimation sequence *E* of length |T| will be generated for the test set T. Linear regression will be used to correlate sequence *E* and the actual fault diagnostic coverage number sequence *A*. That way, the fault diagnostic coverage will be estimated quickly and accurately.

We will use a linear regression approach as in [3] to derive the statistical correlation value *r*, and determine the confidence of the approach for security in automotive and industrial applications. As in [3], we will consider various small cardinality test sets of *n* test patterns. The size of *n* will be small enough to allow for explicit fault simulation so that the best fit line for linear regression is computed [3].

Let $E_i$ and $A_i$ denote the $i^{th}$ numbers in the estimated and actual number sequences by the test set. Let $\bar{E}$ and $\bar{A}$ denote the respective mean values, $\sigma_E$ and $\sigma_A$ the respective standard deviations, and $cov(E, A)$ the covariance of the two number sequences of size *n*. Then the correlation coefficient *r* for the best fit line is calculated as:

$$r = \frac{cov(E,A)}{\sigma_E \sigma_A} = \frac{\sum_{i=1}^{n}(E_i - \bar{E}) \times (A_i - \bar{A})}{\sqrt{\sum_{i=1}^{n}(E_i - \bar{E})^2} \times \sqrt{\sum_{i=1}^{n}(A_i - \bar{A})^2}}$$

Once *r* is derived, the constants for linear regression will be calculated, and the fault diagnostic coverage of the *n* patterns will be estimated. In order to have confidence in *r*, residual values for the training set must be calculated as in [3]. The residuals are defined as the difference between actual and estimated fault diagnostic coverages when considering the *n* test patterns. For each set of *n* patterns, the residuals must have zero mean, constant variance, and must be uncorrelated [3].

In order to have confidence in automotive and industrial applications, the approach must be robust for any small set of *n* test patterns, i.e., the estimated final fault diagnostic coverage must be practically invariant to any derived best fit line for this test set. The fault diagnostic coverage should either be exact or a very close underestimate of the

actual fault diagnostic coverage. Once the selected metric has been verified to be robust, we will use the method to estimate accurately and fast the fault diagnostic coverage of any large size test set T that determines the integrity level in industrial and automotive applications.

The described metric may need to be enhanced appropriately in order to be robust. Any enhancement will focus on more accurate estimate of fault propagation probabilities. Let us for simplicity consider a single stuck-at fault that is activated at the output of a module. In this case, the successive module observes only one error. The ratio of zero to one values at the inputs of the successor module may be used to estimate more accurately the probability of propagating the error through that module. An evaluation on whether such enhancements to the metric are needed will start taking place towards the end of the first half of the proposed project duration, once a working prototype of the fault grading tool has been developed.

The approach will be evaluated on existing benchmarks available to the academia as well as benchmarks provided to the investigators by the sponsor member company. Thorough statistical analysis will be performed to ensure that the approach is robust and meets industrial and automotive standards.

Once a robust framework has been demonstrated, we will enhance the software tool to consider complex clocking scenarios that arise in RTL-level descriptions. For example, some modules may be temporarily disabled, and different scan chains may feed a module at different clocks. In general, the tool will be enhanced to consider RTL-module specifications as in [1]. Such enhancements in the software tool will take place during summer 2016, during the time period where one PhD student is proposed to intern at the sponsor company. That way, the tool will be more valuable to the sponsor company.

Subsequently, we will focus on a more difficult problem formulation, and we investigate whether the proposed method exhibits more robust behavior for certain types of netlist representations for the RTL module descriptions. This will lead to synthesis recommendations that will boost further the integrity level.

The two PIs have extensive research experience in VLSI test and verification, and have collaborated in many research projects. Two PhD students will be working on this research project under the supervision.

**NOVELTY:**

(a) A new metric quantity for the problem under investigation.
(b) The statistical evaluation framework for the proposed metric.

**POTENTIAL BENEFITS TO INDUSTRY MEMBERS:**

1. A fast and accurate grading tool to estimate the quality of a given test set in order to assess whether automotive and industrial safety standards have been met.

2. Thorough experimental evaluation on industrial benchmarks provided by the sponsor company.

**DELIVERABLES:**

1. Scalable software tool to perform accurate RTL-fault grading.
2. Detailed experimental evidence on benchmarks provided by the sponsor company.
3. Determine whether there exist netlist properties that support RTL metric-based accurate simulation.
4. Detailed report and documentation.

**TIMELINE/MILESTONES: (PER QUARTER)**

**First half:**

- Software tool that operates on simple benchmark descriptions.
- Survey of existing methods.

**Second half:**

- Enhancement of the software tool to consider more complex RTL objects and certain industrial benchmarks.
- Experimental evidence.
- Study on netlist properties for the problem under investigation.

## TECHNOLOGY TRANSFER:

- Software tools developed during the course of this project will be transferred to the member company.
- Submission to peer-reviewed conference and journals.

## BUDGET:

$50,000. (See justification later in this section.)
It is also requested that one PhD student interns at Intel in summer 2016. (See justification later in this section.)

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The $50,000 will be allocated as follows:

- One PhD student (Pavan Javvaji) will be supported at 50% (maximum allowed amount) for nine months. The PhD Dissertation topic of Pavan Javvaji, the lead PhD student, is in fault simulation. Pavan has excellent software development skills. It is requested that Pavan Javvaji interns at Intel during summer 2016. (May 15, 2016-August 15, 2016.) This internship will be very beneficial for technology transfer.
- A second PhD student will be supported at 25% for 12 months, and will assist Pavan in the software tool development.
- Partial support for the PIs.
- Travel expenses to visit the member company twice during the duration of the project, and present and demonstrate progress.
- Travel expenses to conference venues to present research findings.
- Expenses for conference and journal publications.

## BIBLIOGRAPHY: (ATTACH IN IEEE CONFERENCE OR JOURNAL FORMAT)


[1] S. Park, L. Chen, P. Parvathala, S. Patil, and I. Pomeranz, "A functional coverage metric for estimating the gate-level fault coverage of functional tests", Proceedings of the International Test Conference, IEEE, 2006.

[2] S. Mirkhani and J. A. Abraham, "Fast evaluation of test vector sets using a simulation-based statistical metric," Proceedings of the VLSI Test Symposium, IEEE, 2014.

[3] S. Mirkhani and J. A. Abraham, "EAGLE: A regression model for fault coverage estimation using a simulation-based metric," Proceedings of the International Test Conference. IEEE, 2014.

[4] C. Kumar, F. Maamari, K. Vittal, W. Pradeep, R. Tiwari, and S. Ravi, "Methodology for Early RTL Testability and Coverage Analysis and Its Application to Industrial Designs", Proceedings of the Asian Test Symposium, pp. 125 – 130, IEEE, 2014.

[5] S. Mirkhani, J. A. Abraham, T. Vo, H. Jun, and B. Eklow, "FALCON: Rapid statistical fault coverage estimation for complex designs," Proceedings of the International Test Conference, IEEE, 2012.

[6] Electronic Design Automation – Synthesis, Verification and Test, (Chapter 3, Section 3.2), L.-T. Wang, Y.-W. Chang, and K.-T. (Tim) Cheng, Editors, Morgan Kaufmann Series in Systems on Silicon, ISBN:978-0-12-374364-0, Elsevier 2009.

# SPYROS TRAGOUDAS

## PROFESSIONAL AFFILIATION AND CONTACT INFORMATION

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## EDUCATION

*1986* Diploma (5 years), Computer Engineering and Informatics Department, University of Patras, Greece

*1988* M.S., Erik Jonsson School of Engineering and Computer Science, Computer Science Program, The University of Texas at Dallas, Richardson, TX 75083-0688.

*1991* Ph.D., Erik Johnson School of Engineering and Computer Science, Computer Science Program, The University of Texas at Dallas, Richardson, TX 75083-0688.

## PROFESSIONAL EXPERIENCE

*07/01/12 – current* Professor and Chair, Electrical & Computer Eng. Dept., Southern Illinois University Carbondale

*03/01/09-current* Director, NSF IUCRC on Embedded Systems, SIUC-site.

*07/16/99- current* Professor, Electrical & Computer Eng. Dept., Southern Illinois University Carbondale.

*08/16/98-07/15/99* Associate Professor, Electrical and Computer Engineering Department, University of Arizona.

*08/16/91-08/15/98* Associate Professor, Computer Science Department, Southern Illinois University Carbondale (Assistant Professor until 6/30/96).

*07/01/97-08/15/98* Graduate Program Director, Computer Science Department, Southern Illinois University Carbondale.

*01/03/87-08/14/91* Research/Teaching Assistant, Computer Science Program, School of Engineering and Computer Science, The University of Texas at Dallas, Richardson, TX 75083-0688.

*08/15/86-01/02/87* Systems Analyst, Computer Technology Institute, Patras, Greece.

## RESEARCH INTERESTS

Design and Test Automation for VLSI, Embedded Systems

## RESEARCH SPONSORS

*Direct support:* National Science Foundation, US Navy, SAIC, Intel, Qualcomm, Synopsys

*NSF IUCRC:* NSF, NAVSEA Crane, Rockwell Collins, United Technologies Aerospace Systems, Ford, SAIC, Intel, Caterpillar, TSI, EMAC, Wildlife Materials

## PROFESSIONAL SERVICE

*Editorial Board:* IEEE Transactions on Computers, VLSI Design journal, Journal of electrical and Computer Engineering, Universal Computer Science, Research Letters in Electronics.

General Chair of IEEE DFTS 2010, Program Committee Chair of DFTS 2009, Program Committee member of many International Conferences

Has graduated 14 PhD students and supervised over 60 MS theses. Currently advising 11 PhD students

## PUBLICATIONS

Over 75 journal papers and over 150 articles in peer-reviewed conference proceedings

*Ten relevant publications*

• J. Lenox and S. Tragoudas, Adapting an Implicit Path Delay Grading Method for Parallel Architectures, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), pp. 1965 - 1976, vol. 33, no. 12, December 2014.

• R. Adapa, S. Tragoudas, and M.K. Michael, Improved diagnosis using enhanced fault dominance, Integration, the VLSI journal, vol. 44, issue 3, pp. 217-228, June 2011.

• S. Gangadhar, S. Tragoudas, An analytical method for estimating SET propagation, Proceedings of the 29th VLSI Test Symposium, pp. 197-202, 2011

• E. Flanigan, S, Tragoudas, Path Delay Measurement Techniques using Linear Dependency Relationships, IEEE Transactions on VLSI Systems, vol. 18, issue 6, pp.1011-1015, June 2010.

• R. Adapa, S. Tragoudas, Techniques to Prioritize Paths for Diagnosis, IEEE Transactions on VLSI Systems, vol. 18, issue 4, pp. 658-661, April 2010.

• D. Jayaraman, E. Flanigan, S. Tragoudas, Implicit Identification of Nonrobustly Testable Unsensitizable Paths using the Bounded Delay Model, Proc. of the IEEE International Test Symposium, pp. 1-10, 28-30 Oct. 2008.

• M.M.V. Kumar and S. Tragoudas, High Quality Transition Fault ATPG for Small Delay Defects, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD). vol. 26, no. 5, pp. 983-989, May 2007.

• R. Adapa, S. Tragoudas, and M.K. Michael, Accelerating Diagnosis via Dominance Relations between Sets of Faults, Proceedings of the 25th IEEE VLSI Test Symposium, pp. 219-224, Session 6.B, Berkeley, CA, May 2007.

• J. Deodhar and S. Tragoudas, Implicit Deductive Fault Simulation for Complex Delay Fault Models IEEE Transactions on VLSI Systems, vol. 12, no. 6, pp. 636-641, June 2004.

• S. Padmanaban, M.K. Michael, and S. Tragoudas, Exact Path Delay Fault Coverage with Fundamental ZBDD Operations, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), vol. 22, no. 3, pp. 305-316, 2003.

# THEMISTOKLIS HANIOTAKIS

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## EDUCATION

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| Ph.D. | [1998] | Department of Informatics, University of Athens, Greece |
| Bachelor | [1991] | Department of Physics, University of Athens, Greece |

## PROFESSIONAL EXPERIENCE

| | |
|---|---|
| [Fall Semester 2013] | Associate Professor, Department of Electrical and Computer Engineering, Southern Illinois University at Carbondale. |
| [2011- Spring 2013] | Tenured Assistant Professor Department of Computer Engineering and Informatics, University of Patras, Greece |
| [Fall Semester 2011] | Sabbatical leave as a Visiting Assistant Professor, Department of Electrical and Computer Engineering, Southern Illinois University at Carbondale. |
| [2007-2011] | Assistant Professor Department of Computer Engineering and Informatics, University of Patras, Greece |
| [2001-2007] | Assistant Professor Department of Electrical and Computer Engineering, Southern Illinois University at Carbondale. |
| [2000-2001] | Visiting Assistant Professor Department of Electrical and Computer Engineering, Southern Illinois University at Carbondale. |
| [1999-2000] | Visiting Assistant Professor Department of Computer Engineering and Informatics, University of Patras, |
| [1998-1999] | Engineer, Low Power & Low Voltage group, ISD Corp. Greece. |
| [1996-1997] | Served in the Greek army. |
| [1991-1995] | Research Center “Demokritos”, Institute of Informatics & Telecommunications, Greece. |

## RESEARCH INTERESTS

VLSI Design & Test, Low-Power & RF VLSI Design

## RESEARCH SPONSORS

European Union/Greek government, Intel, Qualcomm.

## PROFESSIONAL SERVICE

Program Committee member for International On-Line Testing Workshop [2000-2002] International On-Line Testing Symposium [2003-2007], Asia Symposium on Quality Electronic Design ASQED [2010-2013].
Reviewer for numerous Conferences and Journals.
Has supervised 12 MS Thesis.

## PUBLICATIONS

20 journal papers and over 45 articles in peer-reviewed proceedings

Ten relevant publications


[1] “Fast March Tests for Defects in Resistive Memory”, S. N. Mozaffari, S. Tragoudas, and Th. Haniotakis, Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH’15), July 8-10, 2015, Boston, MA, USA.

[2] “ATPG for Transition Faults of Pipelined Threshold Logic Circuits”, A. Palaniswamy, S. Tragoudas, Proceedings of the 9th IEEE International Conference on Design and Technology of Integrated Systems in nanoscale era (DTIS 2014), 6-8 May 2014, Santorini, Greece

[3] "A unified framework for generating all propagation functions for logic errors and events", M.K. Michael, T. Haniotakis, S. Tragoudas, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume: 23 , Issue: 6 , June 2004, pp.980-986

[4] “Algorithm for generation SIC pairs and its implementation in a BIST enviroment” I. Voyiatzis, T. Haniotakis, C. Halatsis IEE Proceedings Circuits Devices and Systems, Volume 153, Issue 5, October 2006 pp. 427-432.

[5] “Testable Designs of Multiple Precharge Domino Circuits” T. Haniotakis, Y. Tsiatouhas, D. Nikolos, C. Efstathiou. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Volume 15, Issue 4, April 2007 pp. 461-465

[6] “A Current Mode, Parallel, Two-Rail Code Checker” S. Matakias, Y. Tsiatouhas, T. Haniotakis, A. Arapoyanni, IEEE Transactions on Computers. Volume 57, Issue 8, Aug. 2008 pp. 1032-1045

[7] "Domino CMOS SCD/SFS 2-out-of-3 and 1-out-of-3 Code Checkers" Th. Haniotakis, Y. Tsiatouhas, C. Efstathiou and D. Nikolos, “Domino-CMOS Strongly Code Disjpoint and Strongly Fault Secure 2-out-of-3 and 1-out-of-3 Code Checkers”, International Journal of Electronics, vol. 90, no. 2, pp. 145-158, 2003.

[8] "A Circuit for Concurrent Detection of soft and Timing Errors in Digital CMOS ICs” S. Matakias, Y. Tsiatouhas, A. Arapoyanni and Th. Haniotakis, Journal of Electronic Testing: Theory and Applications 20, pp. 523-531, 2004.

[9] “A Data Capturing Method for Buses on Chip” M. Skoufis, K. Karmakar, S. Tragoudas, T. Haniotakis, IEEE Transactions on Circuits and Systems I: Regular Papers. Volume 57, Issue 7, 2010 pp. 1631-1641.

[10] “A Methodology for Transistor-Efficient Supergate Design” D. Kagaris, T. Haniotakis, IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Volume 15, Issue 4, April 2007 pp. 488-492