Center for Embedded Systems

An NSF Industry/University Cooperative Research Center

Debugging Errors in Failed Functional Test Sequences

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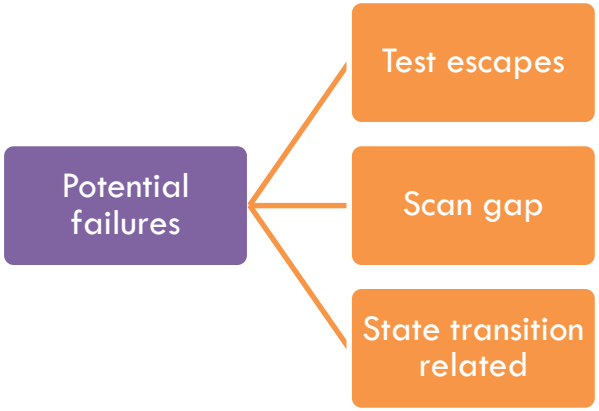
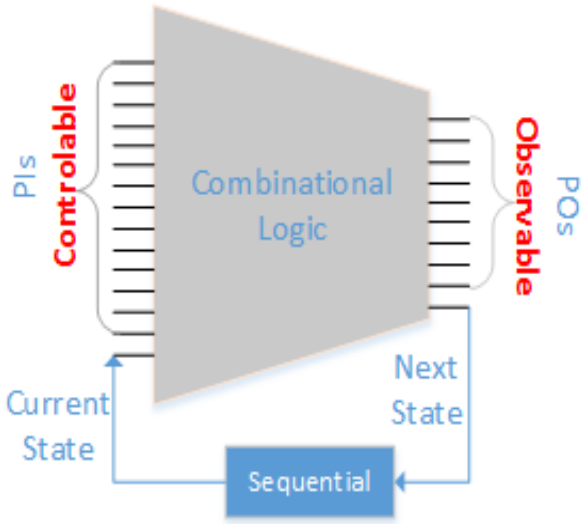
Project Overview and Description

- A formulation for quick diagnosis of the sources of error in a failing system level test
- Approach the problem at a higher level of abstraction like the Register Transfer (RT) level.
- Model error combinations at the outputs of the hierarchical RT level modules



Motivation

- Limited controllability/observability of system level tests
- Labor intensive debug for failed system level tests
- High complexity of gate level ATPG



Approach

- Identify the set of all possible input test sequences for a given output functional sequence using implicit function based methods
- Defect isolation through error analysis on a given set of input and output functional test sequences at the RTL abstraction
- The proposed method provides an error isolation model and in the process generates diagnostic test patterns
- Consider the scenario where a failure may be due to the simultaneous occurrence of multiple errors
- Generated patterns can be applied on ATE or chip level test interfaces such as TAP

Proposed formulation can be modeled using Boolean Satisfiability or Satisfiability Modulo Theories (SMT)

Approach

Novelty

1. Use of implicit function based methods for input sequence generation
2. Isolation of defects independent of fault model
3. Quick defect isolation due to reduced complexity at the RT level abstraction of the circuit
4. Performs multiple error propagation and justification for a more accurate diagnosis of defects

Benefits

1. Effective techniques to avoid the painstaking manual debug of system level test failures
2. Quick defect isolation and diagnostic test generation
3. Effort for pattern generation early in product lifecycle

Project Tasks/ Deliverables

Q1

- Development of techniques to implicitly identify input test sequences using function based methods

Q2

- Implement software tool to generate test sequences

Q3

- Development of methodologies to perform defect isolation at the RT level
- Implement software tool to automate defect isolation and generate diagnostic test patterns to distinguishably test potential defects

Q4

- Procure test cases from member companies and demonstrate the capabilities of the proposed approach

Executive Summary

Phase 1:

- Unroll the circuit for a determined bound
  - Based on the longest path in the data dependency tree
- Function based methods to implicitly generate input test sequences that justify a given output sequence.

Phase 2:

- Evaluate each of the available input sequences against the erroneous output and identify suspect modules.
- Examine a single module at each hierarchy by modelling errors on its outputs.
- Modelled errors from a potential defect source must justify the observed erroneous output.