Center for Embedded Systems

An NSF Industry/University Cooperative Research Center

Exploiting 3D IC Platform to Realize Low Power and High Performance Image/Video Processing VLSI Systems

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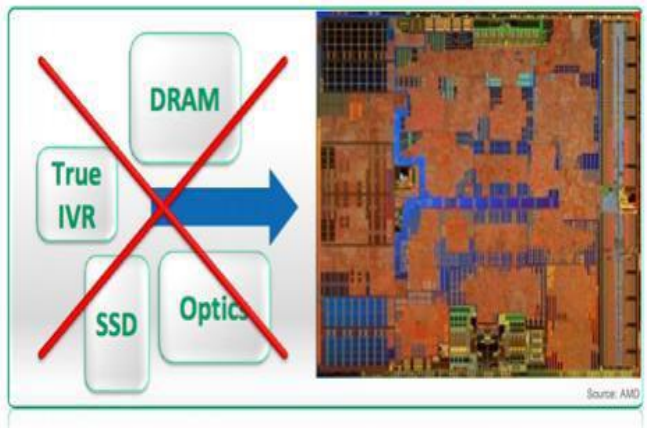
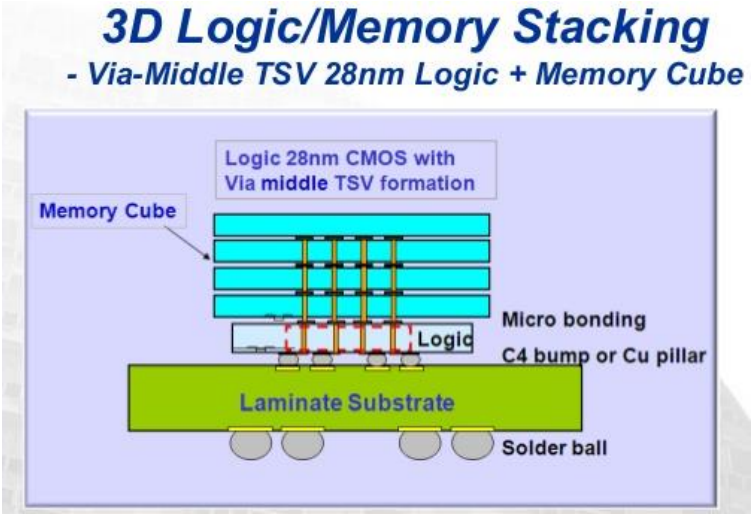
Project Overview

Problem: Existing SOC solutions for future image/video processing do not meet constraints of power, performance, latency, and footprint

SOC: unfriendly integration





Idea: Exploit emerging 3D IC platform to build a 3D memory-in-logic video processor

Approach: **Optimize video processing algorithms and VLSI architecture to meet market demands**

Approach

Novelty: 3D IC is a silicon-proven effective alternative to keep Moore's law, little architecture and algorithm exploration has been done for system optimization

Intel will move away from silicon at 7nm. To keep up with Moore's law, Intel is looking at new materials, 3D packaging.

- from ISSCC 2015

Benefits:

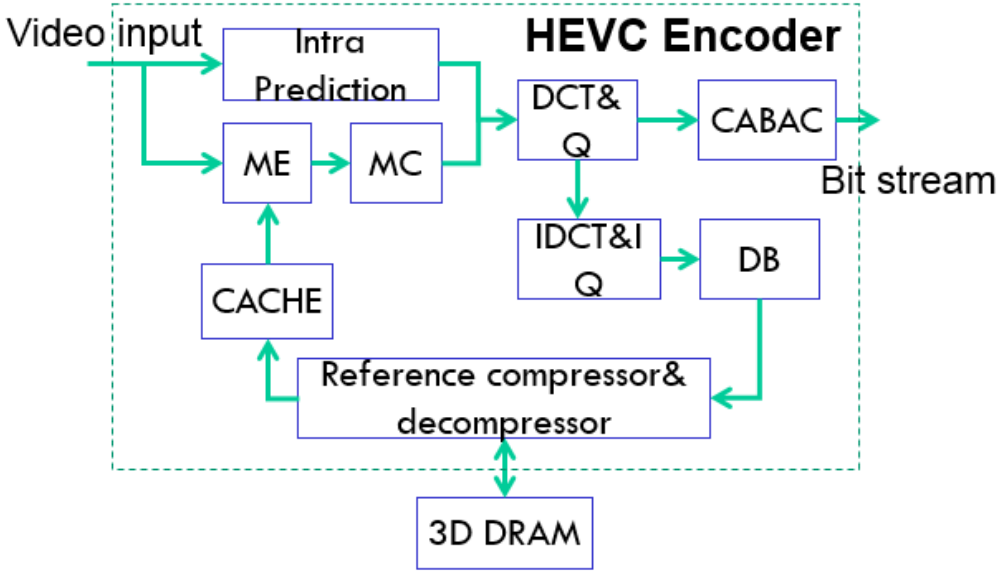
(1) A comprehensive case study of shifting SOC computation systems into future 3D IC platform

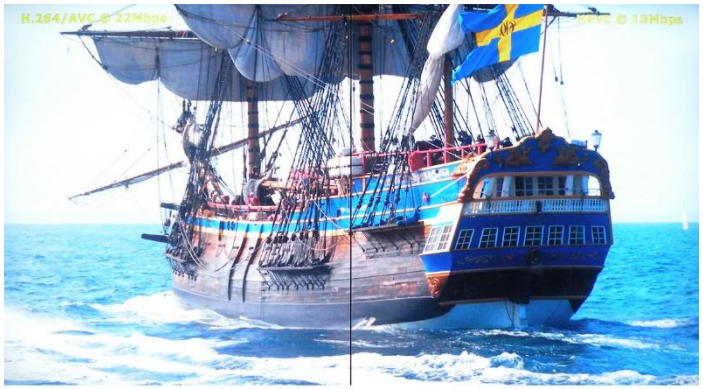
(2) VLSI implementation of a 3D memory-in-logic video processor (prototype demonstration if time permits)

(3) Research outcomes are applicable to other computation and memory-access hungry applications

Project Tasks/ Deliverables

	Description	Date	Status
1	Design of new image/video processing algorithm and VLSI architecture	08/2015-12/2015	
2	VLSI implementation of entire system and design evaluation/demonstration	12/2015-07/2016	

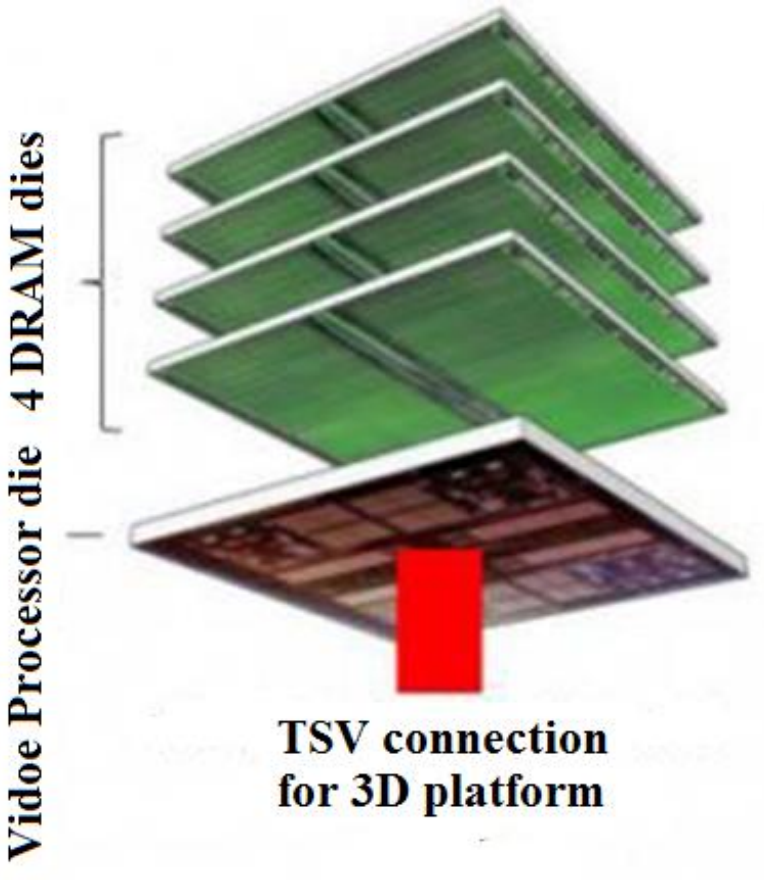




H.264/AVC @ 22Mbps HEVC @ 13Mbps

Executive Summary

- **3D is required for new levels of performance and power**
- **3D does what More Moore can't**
- **It is not just about new manufacturing technology**
  - Its new design
  - Its new architecture
  - Its new algorithm



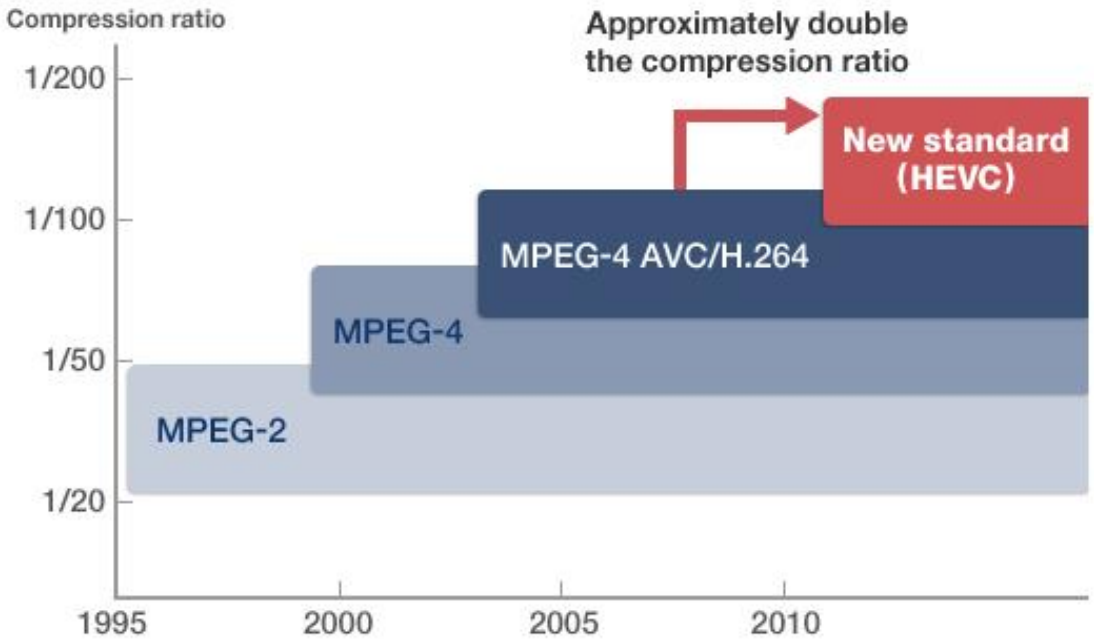
High Efficient Video Coding (HEVC)

- **Next generation of video coding standard**
  - **HD video in mobile devices (tablets, smart phones)**
  - **Require sophisticated architectures and algorithms to double compression rates for same video quality**

Difficulties:

(1) Limited communication bandwidth to support Full HD(1080p) or Ultra HD(4K) video transmission

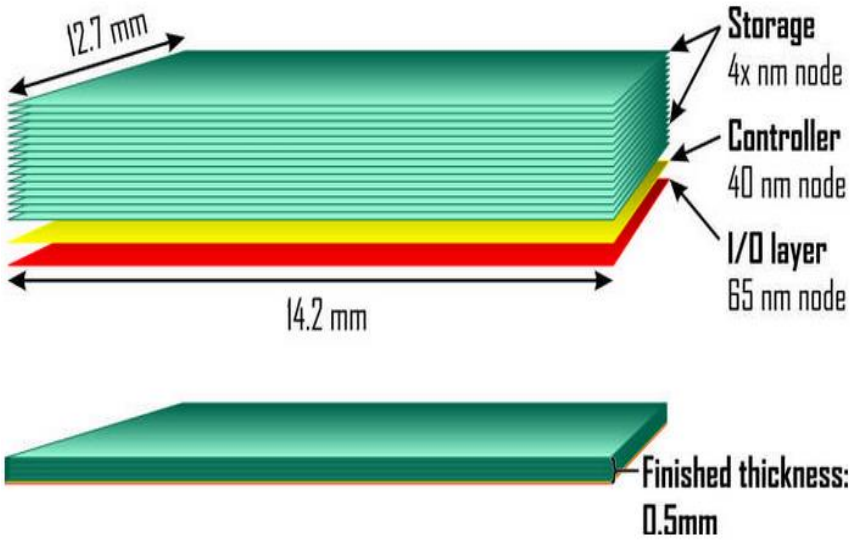
(2) High performance video processor needs a high throughput DRAM, but always leads to larger power consumption and thermal removal problem



3D IC Memory-in-Logic Platform

3D DRAM has been silicon proven by industry

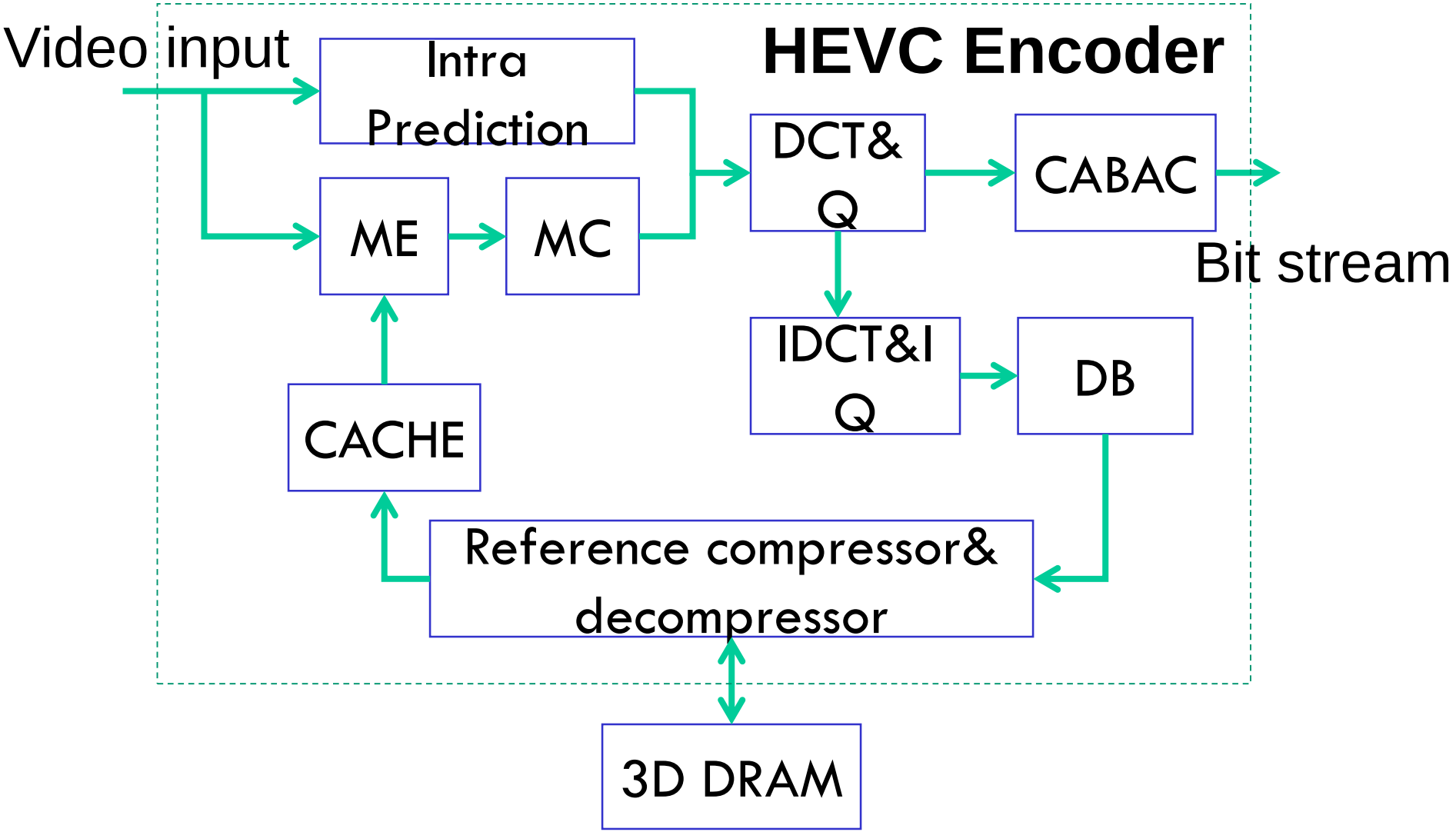
- **Example: Tezzaron DiRAM4 Product**



Product Overview	
Fabrication Process	GF 40nm
Total Capacity	1G bits/die
Clock Frequency	1GHz
Refresh Rate	64ms
# of Data Channel	8
Data Width/Channel	128 bits
Protocol	DDR
Total Data Bandwidth	2Tb/s

3D DRAM stacking is used to provide high data throughput and reduce power consumption

HEVC Algorithm and VLSI Architecture



HEVC Algorithm and VLSI Architecture

ME: motion estimation

MC: motion compensation

DCT: discrete cosine transformation

IDCT: inverse discrete cosine transformation

Q: quantization

IQ: inverse quantization

CABAC: entropy coding

(context adaptive binary arithmetic coding)

DB: De-blocking filter

Cache: internal data cache

3D Memory-in-Logic Video Processor

Contribution:

(1) Propose a cost and power efficient HEVC video coding architecture for real-time high performance applications

(2) Optimize and implement new algorithms in key blocks, such as intra prediction, motion estimation/compensation, entropy coding, 3D denoise, reference frame compression.