Center for Embedded Systems
An NSF Industry/University Cooperative Research Center

Center for Embedded Systems (CES)
Request for Proposals Template – YEAR 7

DUE: Wednesday, April 1, 2015, by 11 p.m.

TITLE:	Exploiting 3D IC Platform to Realize Low Power and High Performance Image/Video Processing		
PI:	Chao Lu	**EMAIL: eeluchao@gmail.com**	**TEL:** 765-491-5604
DEPT:	ECE	**SCHOOL: Southern Illinois University Carbondale**	

ABSTRACT: (250 OR FEWER WORDS)

Enabled by the emerging three-dimensional (3D) integration technologies, 3D stacked IC has a great potential of extending the Moore's low into nanoscale era and realizing next-generation embedded computing systems [1]. Since the 3D IC memory family became standard in 2013 [2] and logic-in-memory products will be available in market in 2015 [3-5], it is increasingly feasible and very attractive to design full embedded computing systems in 3D IC platform. With the great features of 3D IC platform, it is potential to design and realize advanced embedded computing (such as image processing) within the constraints and requirements of power, performance, latency and footprint.

In the proposed research, the motivation is to fully explore 3D IC hardware platform and to achieve low-power, high-quality, and energy-efficient image/video processing. We focus on architecture & algorithm level innovation, as well as system implementation of advanced image processing in 3D IC logic-in-memory platform. The outcomes of this research include: (1) new image processing architecture & algorithm, (2) entire system implementation and design evaluation.

PROBLEM:

Low-power, high-performance, and low-latency are expected in next-generation embedded computing systems, such as image processing. Existing SOC hardware approaches are difficult to meet all the end-user requirements, such as multi-channel I/O, low-latency, large image sizes, high frame rates, small system footprint, and low power consumption. The emerging 3D stacked logic-in-memory hardware is an attractive and increasingly feasible option of embedded computation platform, which enables high memory density (X6), large energy savings (X5), high memory bandwidth (4TB/s), and small system footprint (X8). With these great features of 3D stacked IC, it is potential to design and realize advanced embedded computing (such as image processing) within the constraints and requirements of power, performance, latency and footprint.

Since the state-of-art of 3D IC stacked logic-in-memory system has been presented recently [6-8], the proposed research aims to explore architecture and algorithm level innovation of image processing in the 3D stacked logic-in-memory platform. We will explore and develop new data storage and management algorithms for motion estimation, which is a critical block in next-generation high efficiency video coding (HEVC). Through a case study, we plan to demonstrate how 3D IC logic-in-memory platform benefits embedded computing and enables low-power, low latency and high performance image/video processing tasks.

RATIONALE:

Image/video processing involves frequent data access to memory, and is very sensitive to memory capacity and bandwidth. As a result, image processing tends to perform poorly on conventional SOC embedded systems due to very limited on-chip cache and high cache miss rate. To attack this memory bottleneck problem, one alternative approach is to increase the number and size of on-chip caches. However, this method leads to significant increase of system cost, and is not widely adopted in industry due to unaffordable cost overhead. Another potential approach to address these challenges requires to co-optimize the algorithm, architecture and hardware. This is the focus of this proposal. 3D dense memory [4] integrated with logic enables large memory capacity and fast access time with low cost benefit. Developing image processing algorithms specialized for this memory-in-logic platform can optimize the system to a level that is impossible with general purpose computing.

APPROACH:

We will revise the image/video processing algorithms to match the underlying 3D memory-in-logic hardware platform and adapt the necessary modeling and design framework. Unlike conventional image processing systems on SoC platform, where the data and instructions are located and stored separately due to the limit of on-chip cache. Our proposed design technique will leverage the intrinsic features of enlarged 3D dense memory capacity and fast memory access latency, and exploit mixed storage of image data and commands for energy-efficient, low complexity, real time image/video processing.

NOVELTY:

3D IC hardware platform is a new emerging approach to reduce the power consumption of SoC embedded systems. The proposed work helps explore architecture & algorithm-level design techniques, hence advances the state of the art of next-generation of low-power, high-performance and energy-efficient image/video processing.

POTENTIAL BENEFITS TO INDUSTRY MEMBERS:

The proposed project will be a preliminary study and example of shifting current SoC embedded computation systems into future 3D IC hardware platform. The proposed project will result in significant reduction of hardware cost and improvement of energy efficiency in image/video processing systems. The proposed design techniques are also applicable to other computation and memory-hungry applications in 3D IC platform.

DELIVERABLES:

1. Design of new image processing architecture and algorithm
2. Entire system implementation and design evaluation

TIMELINE/MILESTONES: (PER QUARTER)

Term	Deliverable
August-December	Research and design of the new image processing architecture and algorithm
December-January	System implementation, design simulation and evaluation

TECHNOLOGY TRANSFER:

Technology transfer will be performed in the form of the evaluation tool and comprehensive reports.

BUDGET:

Professional Staff: Chao Lu $9,680/mo for 2 mo $ 19,360
Other Personnel: Graduate Assistant $3,328/mo for 12 mos @ 50% $ 19,968
Fringe Benefits for Professional Staff @ 47.9% $ 9,274
Primary Care Fee for Graduate Assistant $ 291
Travel: Midterm Meeting in AZ $ 763 (Air $300, Mileage $0.56/mi* 234 mi, Lodging $150/night *2 night, $32 per-diem *1 day)
Annual Meeting in MO $ 259 (Mileage $0.56/mi* 234 mi, Lodging $100/night *1 night, $28 per-diem *1 day)

Total Cost $49,915

BIBLIOGRAPHY: (ATTACH IN IEEE CONFERENCE OR JOURNAL FORMAT)

[1] S. Wong, “The Prospect of 3D-IC”, IEEE Custom Integrated Circuits Conference, pp. 445-449, 2009.
[2] W. Shen, “Transition from 2D to 3D IC Design: Advantage, Challenge and Solutions”, Keynote Speech, TSMC, 2013.
[3] Tezzron Presentation, “True 3D Memory Architecture Yields Amazing Performance”, available at http://www.memcon.com/pdfs/proceedings2013/track3/True_3D_Memory_Architecture_Yields_Amazing_Performance.pdf
[4] Tezzaron DiRAM4 Product, available at http://www.tezzaron.com/products/diram4-3d-memory/
[5] Invensas Presentation, “Real 3D IC Solutions” available at http://www.invensas.com/Company/Documents/Invensas_IPCAPEX2013_3D.pdf
[6] Y. Li, “Exploiting Three Dimensional (3D) Memory Stacking to Improve Image Data Access Efficiency for Motion Estimation Accelerators”, Signal Processing: Image Communication, vol. 25, issue 5, pp. 335-344, June, 2010.
[7] Q. Zhu, “Accelerating Sparse Matrix-Matrix Multiplication with 3D Stacked Logic-in-Memory Hardware”, IEEE High Performance Extreme Computing Conference, pp. 1-6, 2013.
[8] Q. Wu, “Design Techniques to Facilitate Process Power Delivery in 3D Processor DRAM Integrated Systems”, IEEE Transactions on VLSI Systems, vol. 19, no. 9, pp. 1655-1666, September 2011.

PI INFORMATION: (ATTACH 2-PAGE CV)

Chao Lu
Department of Electrical and Computer Engineering
Southern Illinois University, Carbondale, IL, 62901-6603
Phone: (765) 491-5604; Email: eeluchao@gmail.com

Professional Preparation:

Purdue University, West Lafayette, IN	Ph.D.	Electrical and Comp. Engineering	12/12
Hong Kong Univ. of Science & Technology	M. Eng.	Electrical and Comp. Engineering	07/07
Nankai University, Tianjin, China	B. Eng.	Microelectronics	05/04

Professional Experience:

08/15-Present	Assistant Professor, Department of Electrical and Computer Engineering, Southern Illinois University (SIU), Carbondale, IL 62901
09/14-08/15	3D IC Chip Designer, Tezzaron Semiconductor, IL, 60563
01/13-09/14	R&D Circuit Design Engineer, Arctic Sand Technologies, Cambridge, MA
08/08-12/12	Research Assistant, Department of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906
05/11-08/11	Intern Engineer, Silicon Laboratories Inc., Sunnyvale, CA, 94085
08/05-08/07	Research Assistant, Department of Electrical and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong, China
08/04-08/05	Teaching Assistant, Department of Electrical and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong, China

Research Interests:

- 3D IC Design, Modelling and System Optimization
- Device/Circuit/Architecture/Algorithm/System Co-Design and Joint Optimization
- Energy Harvesting and Analog Power Management IC Design

Honors and Awards:

- Best paper award, ACM International Symposium on Low-Power Electronics and Design 2007

Professional Service:

- Technical Program Committee of ACM International Symposium on Low-Power Electronics and Design, 2015, Los Angeles, CA
- Technical Program Committee of IEEE/ACM Great Lake Symposium on VLSI, 2011-2014
- Editorial Board Member of International Journal of Electronics and Communications, Elsevier, 2012-Present
- Journal Referee
    - IEEE Journal of Solid-State Circuits (JSSC)
    - IEEE Transactions on Very Large Scale Integration (VLSI) Systems
    - IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)
    - IEEE Transactions on Circuits and Systems I (TCAS-I)
    - IEEE Transactions on Circuits and Systems II (TCAS-II)
    - IEEE Transactions on Computers (TC)
    - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)

- IEEE Embedded System Letters(ESL)
- IEEE Transactions on Mobile Computing (TMC)
- IEEE Design & Test of Computers
- Microelectronics Journal
- ACM Journal of Emerging Technologies in Computing (JETC)
- ACM Transactions in Embedded Computing Systems (TECS)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)

Recent Publications:

1. S. Baytok, C. Lu, C. H. Ho, V. Raghunathan, K. Roy, "Effects of Deposition Process on Poly-Si Micro-scale Energy Scavenging Systems", IEEE Transactions on Electron Devices, under review.
2. C. H. Ho, C. Lu, K. Roy, "An enhanced voltage programming pixel circuit for compensating brightness variation in AMOLED displays", IEEE Journal of Display Technology, vol. 10, issue 5, pp. 345-351, January, 2014.
3. C. Lu, C. Y. Tsui, W. H. Ki, "Vibration energy scavenging system with maximum power tracking for micro power applications", IEEE Transactions on VLSI Systems, vol. 19, issue 11, pp. 2109-2119, November, 2011.
4. C. Lu, V. Raghunathan, K. Roy, "Efficient design of micro-scale energy harvesting systems", IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 1, issue 3, pp. 254-266, September, 2011.
5. C. W. Lin, C. H. Ho, C. Lu, D. Fang and K. Roy, "A process/device/circuit/system compatible simulation framework for poly-Si TFT based SRAM design", SISPAD, 2013.
6. S. H. Choday, C. Lu, V. Raghunathan, K. Roy, "On-chip energy harvesting using thin-film thermoelectric materials", Semi-Therm, 2013.
7. C. H. Ho, G. D. Panagopoulos, C. Lu, K. Roy, "A physical model to predict the vth variation of poly-si TFTs induced by grain boundaries", SISPAD, 2012.
8. S. Baytok, C. Lu, K. Roy, V. Raghunathan, "Modeling, design and cross-layer optimization of polysilicion solar cell based micro-scale energy harvesting system", ISLPED, 2012.
9. C. Lu, S. P. Park, V. Raghunathan, K. Roy, "Low overhead maximum power point tracking for micro-scale solar energy harvesting systems", VLSI Design, 2012.
10. C. Lu, S. P. Park, V. Raghunathan, K. Roy, "Stage number optimization for switched capacitor power converter in micro-scale energy harvesting", DATE, 2011.
11. C. H. Ho, C. Lu, D. Mohapatra and K. Roy, "Variation-tolerant and self-repair design methodology for low temperature polycrystalline silicon liquid crystal and organic light emitting diode displays", ASPDAC, 2011.
12. C. Lu, V. Raghunathan, K. Roy, "Maximum power point considerations for micro-scale solar energy harvesting systems", ISCAS, 2010. (Invited)
13. C. Lu, V. Raghunathan, K. Roy, "Micro-scale energy harvesting: a system perspective", ASPDACP, 2010. (Invited)
14. C. Lu, S. P. Park, V. Raghunathan, K. Roy, "Analysis and design of ultra-low power thermoelectric energy harvesting systems", ISLPED, 2010.
15. C. Lu, S. P. Park, V. Raghunathan, K. Roy, "Efficient power conversion for ultra-low voltage micro scale energy transducers", DATE, 2010.
16. C. Lu, C. Y. Tsui, W. H. Ki, "Vibration energy scavenging and management for ultra-low power Applications", ISLPED, 2007 (Best Paper Award, 2 out of 192 submissions, 1%)
17. C. Lu, C. Y. Tsui, W. H. Ki, "A batteryless vibration-based energy harvesting system for ultra-low power ubiquitous applications", ISCAS, 2007.

I/UCRC Executive Summary - Project Synopsis			Date: 03/31/2015
Project Title: **Exploiting 3D IC Platform to Realize Low Power and High Performance Image/Video Processing**			
Center/Site: Center for Embedded Systems/Southern Illinois University Carbondale			
Principle Investigator: Chao Lu			**Type: (New or Continuing)**
Tracking No.: (CES office to input)	**Phone : 765-491-5604**		**E-mail : eeluchao@gmail.com**
			Proposed Budget: $50,000

Abstract: Enabled by the emerging three-dimensional (3D) integration technologies, 3D stacked IC has a great potential of extending the Moore's low into nanoscale era and realizing next-generation embedded computing systems. Since the 3D IC memory family became standard in 2013 and logic-in-memory products will be available in market in 2015, it is increasingly feasible and very attractive to design full embedded computing systems in 3D IC platform. With the great features of 3D IC platform, it is potential to design and realize advanced embedded computing (such as image processing) within the constraints and requirements of power, performance, latency and footprint.
In the proposed research, the motivation is to fully explore 3D IC hardware platform and to achieve low-power, high-quality, and energy-efficient image/video processing. We focus on architecture & algorithm level innovation, as well as system implementation of advanced image processing in 3D IC logic-in-memory platform. The outcomes of this research include: (1) new image processing architecture & algorithm, (2) entire system implementation and design evaluation.

Problem: Low-power, high-performance, and low-latency are expected in next-generation embedded computing systems, such as image processing. Existing SoC hardware approaches are difficult to meet all the end-user requirements, such as multi-channel I/O, low-latency, large image sizes, high frame rates, small system footprint, and low power consumption. The emerging 3D stacked logic-in-memory hardware is an attractive and increasingly feasible option of embedded computation platform, which enables high memory density (X6), large energy savings (X5), high memory bandwidth (4TB/s), and small system footprint (X8). With these great features of 3D stacked IC, it is potential to design and realize advanced embedded computing (such as image processing) within the constraints and requirements of power, performance, latency and footprint.
Since the state-of-art of 3D stacked logic-in-memory IC has been presented recently in industry, the proposed research aims to explore architecture and algorithm level innovation of image processing in the 3D stacked logic-in-memory platform. We will explore and develop new data storage and management algorithms for motion estimation, which is a critical block in next-generation high efficiency video coding (HEVC). Through a case study, we plan to demonstrate how 3D IC logic-in-memory platform benefits embedded computing and enables low-power, low latency and high performance image/video processing tasks.

Rationale / Approach: To address these challenges of image/video processing, our approach is to co-optimize the algorithm, architecture and hardware. We will revise the image/video processing algorithms to match the underlying 3D memory-in-logic hardware platform and adapt the necessary modeling and design framework.

Novelty: 3D IC hardware platform is a new emerging approach to reduce the power consumption of SoC embedded systems. The proposed work helps explore architecture & algorithm-level design techniques, hence advances the state of the art of next-generation of low-power, high-performance and energy-efficient image/video processing.

Potential Member Company Benefits: The proposed project will be a preliminary study and example of shifting current SoC embedded computation systems into future 3D IC hardware platform. The proposed project will result in significant reduction of hardware cost and improvement of energy efficiency in image/video processing systems. The proposed design techniques are also applicable to other computation and memory-hungry applications in 3D IC platform.

Deliverables for the proposed year: 1. Design of new image processing architecture and algorithm
2. Entire system implementation and design evaluation

Milestones for the proposed year: Q1: Exploration of existing research in the area of 3D IC memory-in-logic platform, Q2: Select a set of image/video processing algorithms, Q3: Implement and optimize image processing algorithms on 3D IC memory-in-logic platform, Q4: entire system implementation and evaluation

Progress to Date: **THIS SECTION TO BE UPDATED IN JANUARY**

Estimated Start Date: August 16 2015	**Estimated Knowledge Transfer Date**: August 15 2016