I/UCRC Executive Summary - Project Synopsis		Date: 03/31/2015
Project Title:	**Debugging Errors in Failed Functional Test Sequences**	
Center/Site: NSF I/UCRC for Embedded Systems, SIUC site		
Principle Investigators: Spyros Tragoudas, Themistoklis Haniotakis		**Type: New**
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		Proposed Budget: $50,000

Abstract:
Proposed is a formulation for quick diagnosis of the sources of failure in a failing system level test when functional input sequences are applied. The formulation tries to determine the possible combinations of multiple defects in the device that justify the observed output error sequence. These failures may correspond to one of the following: defects that escaped structural tests, defects in the untested parts of the circuit that lack scan coverage (shadow logic around SRAM), functional defects that are triggered only when particular sequence of input is applied.

Problem:

1. Identify the set of all possible input test sequences for a given output functional sequence using implicit function based methods
2. Defect isolation in integrated circuits by performing error analysis on a given set of input and output functional test sequences at the RTL abstraction of integrated circuits

Rationale / Approach:

1. Traditional ATPG methods fail to detect many potential defects in the increasingly complex modern integrated circuits
2. The process of debugging defects emanating during system level tests involves intensive manual labor and time. This makes it challenging to achieve the ever shrinking time-to-market.
3. Scalability issues diagnosis at the gate level are alleviated by approaching the problem at a higher level of abstraction like the Register Transfer (RT) level.
4. The approach works by modeling error combinations at the outputs of the hierarchical RT level modules and propagating the errors to justify the observed erroneous output.

Novelty:

1. Use of implicit function based methods in identifying the set of all possible input test sequences corresponding to a given output sequence
2. Isolation of defects independent of fault model
3. Quick defect isolation due to reduced complexity at the RT level abstraction of the circuit

Potential Member Company Benefits:

1. Effective techniques to avoid the painstaking manual debug of system level test failures
2. Quick defect isolation and diagnostic test generation

Deliverables for the proposed year:

1. Software tool to implicitly identify input test sequences using function based methods
2. Software tool to perform defect isolation and diagnostic test generation at the RT level

Estimated Start Date: 08/16/2015	**Estimated Knowledge Transfer Date**: 08/16/2016

Center for Embedded Systems (CES)
Request for Proposals Template – YEAR 7

TITLE:	**Debugging Errors in Failed Functional Test Sequences**				
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ABSTRACT: (250 OR FEWER WORDS)

Proposed is a formulation for quick diagnosis of the sources of failure in a failing system level test when functional input sequences are applied. The formulation tries to determine the possible combinations of multiple defects in the device that justify the observed output error sequence. These failures may correspond to one of the following: defects that escaped structural tests, defects in the untested parts of the circuit that lack scan coverage (shadow logic around SRAM), functional defects that are triggered only when particular sequence of input is applied.

PROBLEM:

1. Identify the set of all possible input test sequences for a given output functional sequence using implicit function based methods
2. Defect isolation in integrated circuits by performing error analysis on a given set of input and output functional test sequences at the RTL abstraction of integrated circuits

RATIONALE:

1. Traditional ATPG methods fail to detect many potential defects in the increasingly complex modern integrated circuits
2. Certain defects may be triggered only during the execution of particular input instruction sequences. Such defects cannot be detected using structural debug techniques
3. Defects triggered at extreme sequential depths may escape manufacturing tests but cause the system level executions to crash
4. The process of debugging defects emanating during system level tests involves intensive manual labor and time. This makes it challenging to achieve time-to-market requirements.

APPROACH:

One approach to debug failures observed during system level testing is to analyze the logic in the circuit that was activated based on the instruction that was issued and generate functional test patterns to detect previously uncovered defects in that cone of logic using different fault models. For example, a write or read memory instruction would access the SRAM in the device and based on the address one can identify the cone of logic feeding to a particular SRAM module. Traditionally, such an approach is carried out on the gate level netlist and in many instances this is not scalable due to the vast number of gates in modern designs. Also, one has to assume a fault model and many existing commercial Automatic Test Pattern Generators (ATPG) assume single faults and generate test patterns considering only one of the erroneous output pins at a time. On the other hand, the

proposed approach identifies values at the RT level modules at different hierarchies that justify the values on all pins of the output.

We address such scalability issues by approaching the problem at a higher level of abstraction like the Register Transfer (RT) level. The proposed method provides an error isolation model and in the process generates diagnostic test patterns. The approach works by modeling error combinations at the outputs of the hierarchical RT level modules and propagating the errors to justify the observed erroneous output. By doing so we identify the RT level modules that are the potential source of error and focus our effort on identifying the defect at lower levels of abstraction with in the modules only. This way the complexity is reduced to the size of the smaller modules. Finally, diagnostic patterns are made available to trigger the defects and propagate the effects to the observable outputs.

One of the advantages of such a modeling formulation is that it is not dependent on assuming fault models at the RT level and this, further simplifies the complexity of the proposed approach. Also, in the proposed formulation we consider the scenario where a failure may be due to the simultaneous occurrence of errors on multiple outputs of a module.

The proposed formulation can be modeled using Boolean Satisfiability or Satisfiability Modulo Theories (SMT). Solvers based on SMT can effectively model RT level circuit descriptions written in behavioral and structural Verilog.

Recent work in [1][2] deal with generating functional tests for hard to detect stuck at faults that were not covered by structural tests. The approach in [1][2] assumes a fault model and cannot effectively debug arbitrary defects that result in failed system level tests. [3] addresses the existence of cases where failing circuits are affected by multiple defects. However, the approach in [3] can only be applied to gate level description of circuits and thus, is not scalable for large and complex modern circuits. The problem tackled by [5] is very close to the one addressed by the proposed approach. However, the solution in [5], unlike the proposed solution, is based on reachability analysis of states and requires on-chip support logic.

The proposed formulation consists of two phases. The first phase involves a test generation procedure to implicitly generate input test sequences that justify a given output sequence using function based methods. The second phase deals with isolating the hierarchy at which the error was generated by considering each of the possible input sequences and the erroneous output. In this process we consider a single module at each hierarchy and check to see if an error appearing on the outputs of the module can justify the observed erroneous output. If it does justify the output then the module is considered to be a potential source of the defect or along an error propagation path. The proposed approach is applied by iteratively scaling down the hierarchies until we reach modules small enough to allow for more exhaustive debug.

NOVELTY:

1. Use of implicit function based methods in identifying the set of all possible input test sequences corresponding to a given output sequence
2. Isolation of defects independent of fault model
3. Quick defect isolation due to reduced complexity at the RT level abstraction of the circuit
4. Performs multiple error propagation and justification for a more accurate diagnosis of defects

POTENTIAL BENEFITS TO INDUSTRY MEMBERS:

1. Effective techniques to avoid the painstaking manual debug of system level test failures
2. Quick defect isolation and diagnostic test generation

DELIVERABLES:

1. Software tool to implicitly identify input test sequences using function based methods
2. Software tool to perform defect isolation and diagnostic test generation at the RT level

TIMELINE/MILESTONES: (PER QUARTER)

Q1 and Q2:

- Development of techniques to implicitly identify input test sequences using function based methods
- Implement software tool to generate test sequences

Q3:

- Development of methodologies to perform defect isolation at the RT level
- Implement software tool to automate defect isolation and generate diagnostic test patterns to distinguishably test potential defects

Q4:

- Procure test cases from member companies and demonstrate the capabilities of the proposed approach

TECHNOLOGY TRANSFER:

- Software tools developed during the course of this project will be transferred to the member company.
- Submission to peer-reviewed conference and journals.

BUDGET:

Cost of $50,000

- Support a graduate student for up to 25%.
- Partial support for the PIs.
- Travel to Member Company and conferences to present research findings.

BIBLIOGRAPHY: (ATTACH IN IEEE CONFERENCE OR JOURNAL FORMAT)

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[2] Prabhu, M.; Abraham, J.A., "Application of under-approximation techniques to functional test generation targeting hard to detect stuck-at faults," *IEEE International Test Conference (ITC), 2013,* vol., no., pp.1,7, 6-13 Sept. 2013

[3] Hongxia Fang; Chakrabarty, K.; Jas, A.; Patil, S.; Tirumurti, C., "Functional Test-Sequence Grading at Register-Transfer Level," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol.20, no.10, pp.1890,1894, Oct. 2012

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[5] Bao Le; Sengupta, D.; Veneris, A.; Poulos, Z., "Accelerating post silicon debug of deep electrical faults," *IEEE 19th International On-Line Testing Symposium (IOLTS), 2013*, vol., no., pp.61,66, 8-10 July 2013

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PROFESSIONAL AFFILIATION AND CONTACT INFORMATION

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EDUCATION

1986 Diploma (5 years), Computer Engineering and Informatics Department, University of Patras, Greece

1988 M.S., Erik Jonsson School of Engineering and Computer Science, Computer Science Program, The University of Texas at Dallas, Richardson, TX 75083-0688.

1991 Ph.D., Erik Johnson School of Engineering and Computer Science, Computer Science Program, The University of Texas at Dallas, Richardson, TX 75083-0688.

PROFESSIONAL EXPERIENCE

07/01/12 – current Professor and Chair, Electrical & Computer Eng. Dept., Southern Illinois University Carbondale

03/01/09-current Director, NSF IUCRC on Embedded Systems, SIUC-site.

07/16/99- current Professor, Electrical & Computer Eng. Dept., Southern Illinois University Carbondale.

08/16/98-07/15/99 Associate Professor, Electrical and Computer Engineering Department, University of Arizona.

08/16/91-08/15/98 Associate Professor, Computer Science Department, Southern Illinois University Carbondale (Assistant Professor until 6/30/96).

07/01/97-08/15/98 Graduate Program Director, Computer Science Department, Southern Illinois University Carbondale.

01/03/87-08/14/91 Research/Teaching Assistant, Computer Science Program, School of Engineering and Computer Science, The University of Texas at Dallas, Richardson, TX 75083-0688.

08/15/86-01/02/87 Systems Analyst, Computer Technology Institute, Patras, Greece.

RESEARCH INTERESTS

Design and Test Automation for VLSI, Embedded Systems

RESEARCH SPONSORS

Direct support: National Science Foundation, US Navy, SAIC, Intel, Qualcomm, Synopsys

NSF IUCRC: NSF, NAVSEA Crane, Rockwell Collins, United Technologies Aerospace Systems, SAIC, Intel, Caterpillar, TSI, EMAC, Wildlife Materials

PROFESSIONAL SERVICE

Editorial Board: IEEE Transactions on Computers, VLSI Design journal, Journal of electrical and Computer Engineering, Universal Computer Science, Research Letters in Electronics.

General Chair of IEEE DFTS 2010, Program Committee Chair of DFTS 2009, Program Committee member of many International Conferences

Has graduated 14 PhD students and supervised over 60 MS theses. Currently advising 11 PhD students

PUBLICATIONS

Over 70 journal papers and over 130 articles in peer-reviewed conference proceedings

Ten recent journal publications

• A.K. Palaniswamy and S.Tragoudas, An Efficient Heuristic to Identify Threshold Logic Functions, ACM Journal on Emerging Technologies in Computing (JETC), to appear in 2012.

• M.N. Skoufis, S. Tragoudas, An on-line Failure Detection Method for Data Buses using Multi-threshold Receiving Logic, IEEE Transactions on Computers, vol. 61, no. 2, pp. 187-198, Feb. 2012

• K. Stewart, Th. Haniotakis, and S. Tragoudas, Securing sensor networks: A novel approach that combines encoding, uncorrelation, and node disjoint transmission, Ad Hoc Networks, vol. 10, issue 3, May 2012, pp. 328-328, Elsevier.

• M.N. Skoufis, K. Karmakar, S. Tragoudas, and T. Haniotakis, A data capturing method for buses on chip, IEEE Transactions on Circuits and Systems I, vol. 57, no. 7, pp.1631-1641, July 2010.

• D. Jayaraman, R. Sethuram, and S. Tragoudas, Scan Shift Power Reduction by Gating Internal Nodes. J. Low Power Electronics 6(2): 311-319 (2010).

• E. Flanigan, S, Tragoudas, Path Delay Measurement Techniques using Linear Dependency Relationships, IEEE Transactions on VLSI Systems, vol. 18, issue 6, pp.1011-1015, June 2010.

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• K. Christou, M. K. Michael, and S. Tragoudas, On the Use of ZBDDs for Implicit and Compact Critical Path Delay Fault Test Generation, Journal of Electronic Testing: Theory and Applications, 2008.

• A. Abdulrahman and S. Tragoudas, Low-Power Multi-Core ATPG to Target Concurrency, Integration, the VLSI Design Journal, vol. 41, issue 4, pp. 459-473, July 2008.

• C. Song, S. Tragoudas, Identification of Critical Executable Paths at the Architectural Level, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), vol. 27, no. 12, pp. 2291-2302, December 2008

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EDUCATION

Ph.D.	[1998]	Department of Informatics, University of Athens, Greece
Bachelor	[1991]	Department of Physics, University of Athens, Greece

PROFESSIONAL EXPERIENCE

[Fall Semester 2013]	Associate Professor, Department of Electrical and Computer Engineering, Southern Illinois University at Carbondale.
[2011- Spring 2013]	Tenured Assistant Professor Department of Computer Engineering and Informatics, University of Patras, Greece
[Fall Semester 2011]	Sabbatical leave as a Visiting Assistant Professor, Department of Electrical and Computer Engineering, Southern Illinois University at Carbondale.
[2007-2011]	Assistant Professor Department of Computer Engineering and Informatics, University of Patras, Greece
[2001-2007]	Assistant Professor Department of Electrical and Computer Engineering, Southern Illinois University at Carbondale.
[2000-2001]	Visiting Assistant Professor Department of Electrical and Computer Engineering, Southern Illinois University at Carbondale.
[1999-2000]	Visiting Assistant Professor Department of Computer Engineering and Informatics, University of Patras,
[1998-1999]	Engineer, Low Power & Low Voltage group, ISD Corp. Greece.
[1996-1997]	Served in the Greek army.
[1991-1995]	Research Center “Demokritos”, Institute of Informatics & Telecommunications, Greece.

RESEARCH INTERESTS

VLSI Design & Test, Low-Power & RF VLSI Design

RESEARCH SPONSORS

European Union/Greek government, Intel, Qualcomm.

PROFESSIONAL SERVICE

Program Committee member for International On-Line Testing Workshop [2000-2002] International On-Line Testing Symposium [2003-2007], Asia Symposium on Quality Electronic Design ASQED [2010-2013].
Reviewer for numerous Conferences and Journals.
Has supervised 12 MS Thesis.

PUBLICATIONS

20 journal paper and over 45 articles in peer-reviewed proceedings

Ten Recent journal publications

[1] "Domino CMOS SCD/SFS 2-out-of-3 and 1-out-of-3 Code Checkers" Th. Haniotakis, Y. Tsiatouhas, C. Efstathiou and D. Nikolos, “Domino-CMOS Strongly Code Disjpoint and Strongly Fault Secure 2-out-of-3 and 1-out-of-3 Code Checkers”, International Journal of Electronics, vol. 90, no. 2, pp. 145-158, 2003.

[2] "A unified framework for generating all propagation functions for logic errors and events", M.K. Michael, T. Haniotakis, S. Tragoudas, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume: 23 , Issue: 6 , June 2004, pp.980-986

[3] "A Circuit for Concurrent Detection of soft and Timing Errors in Digital CMOS ICs” S. Matakias, Y. Tsiatouhas, A. Arapoyanni and Th. Haniotakis, Journal of Electronic Testing: Theory and Applications 20, pp. 523-531, 2004.

[4] “A Design Technique for Energy Reduction in NORA CMOS Logic” K. Limniotis, Y. Tsiatouhas, T. Haniotakis A. Arapoyanni, IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications. Volume 53, Issue 12, Dec. 2006 pp. 2647-2655

[5] “Algorithm for generation SIC pairs and its implementation in a BIST enviroment” I. Voyiatzis, T. Haniotakis, C. Halatsis IEE Proceedings Circuits Devices and Systems, Volume 153, Issue 5, October 2006 pp. 427-432.

[6] “A Methodology for Transistor-Efficient Supergate Design” D. Kagaris, T. Haniotakis, IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Volume 15, Issue 4, April 2007 pp. 488-492

[7] “Testable Designs of Multiple Precharge Domino Circuits” T. Haniotakis, Y. Tsiatouhas, D. Nikolos, C. Efstathiou. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Volume 15, Issue 4, April 2007 pp. 461-465

[8] “A Current Mode, Parallel, Two-Rail Code Checker” S. Matakias, Y. Tsiatouhas, T. Haniotakis, A. Arapoyanni, IEEE Transactions on Computers. Volume 57, Issue 8, Aug. 2008 pp. 1032-1045

[9] “A Data Capturing Method for Buses on Chip” M. Skoufis, K. Karmakar, S. Tragoudas, T. Haniotakis IEEE Transactions on Circuits and Systems I: Regular Papers. Volume 57, Issue 7, 2010 pp. 1631-1641.

[10] “Securing sensor networks: A novel approach that combines encoding, uncorrelation and node disjoint transmission”, Khadija Stewart, Themistoklis Haniotakis, Spyros Tragoudas, Ad Hoc Networks, Volume 10, Issue 3, May 2012, Pages 328–338