Group 1

1.5 Towards Predictable Execution of Safety-Critical Tasks on Mixed-criticality Multi-core Platforms, Pis: D. Kagaris, H. Ramaprasad, SIUC

Center for Embedded Systems

An NSF Industry/University Cooperative Research Center

Towards Predictable Execution of Safety-Critical Tasks on Mixed-Criticality Multi-Core Platforms.

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Project Overview and Description

- Project Description
  - Integrate independent High-Safety Sensitive (HSS) and Low-Safety Sensitive (LSS) applications onto one physical computing platform
  - Cost and space effective integration
  - Characterize HSS behavior in presence of LSS tasks
  - Develop cache locking and message passing policies
- Problem
  - Deterministic execution of HSS in the presence of LSS tasks and other HSS tasks is challenging
- Feasible Solution
  - Use modern virtualization (hypervisor) technology to isolate HSS and LSS application on a multi-core platform
  - Use cache locking for HSS tasks for predictable execution times
- Applications
  - Integrate multiple avionics modules in a “single box”

Approach

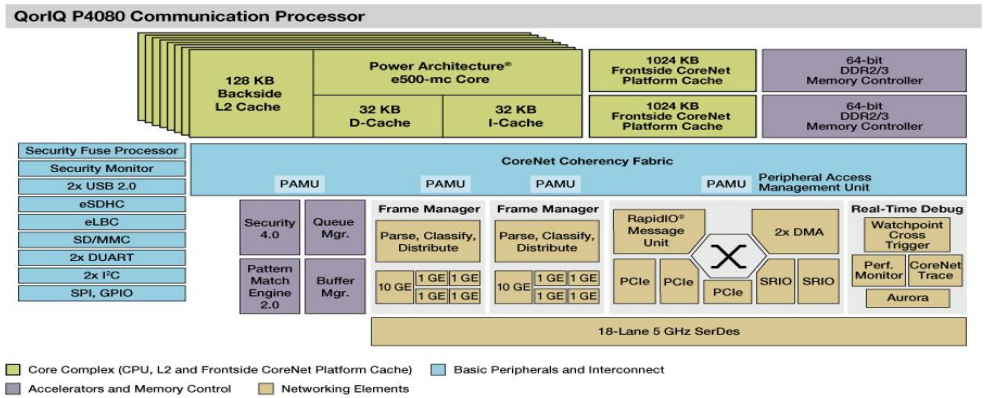
- Two stage approach
  - **Stage 1:**
    - Use cache locking and partitioning to improve predictability of HSS tasks
    - Explore applicability of *minimum utilization* and *minimize interference* policies to end-use scenarios
  - **Stage 2:**
    - Allow one partition to be a “manager” that can *pause, stop, resume other partitions*
      - Dynamically control LSS tasks resource usage during overload situations
      - Efficient power/energy conservation
- Metrics for measuring success of techniques
  - HSS tasks: Determinism
  - LSS tasks: Quality-Of-Service (QoS)
- Novelty
  - No existing research on mixed criticality execution in virtualized environments on P4080 platform
- Potential member company benefits
  - Provide basis for safe execution of mixed-criticality workloads on multi-core architectures with support for virtualization

Project Tasks/ Deliverables

	Description	Date	Status
1	Exploration of existing research in the area of cache locking and partitioning.	Q1	Complete
2	Workload characterization and end-use scenario analysis under cache locking and partitioning schemes.	Q2	Ongoing
3	Exploration of mechanisms to create and configure manager partitions;	Q3	Ongoing
4	Development of strategies for dynamic resource management using manager partitions	Q3	Not yet started
5	Report writing and technology transfer	Q4	Not yet started

Technical Detail

- Freescale QorIQ P4080
  - 8 high-performance cores
    - Private L1 & L2 caches
    - Shared L3 cache



- Embedded hypervisor
  - Safe OS partitioning
  - Takes advantage of hardware mechanisms present in cores
  - Provides support for partitioning cores, memory, I/O devices
    - Each OS *only* accesses resources it is authorized to access
    - Each OS *owns* resources in its partition
    - Partitions are static
  - Can configure one partition as "*manager partition*"
  - External interrupts may be directly sent to Oss

- High-bandwidth communication & coherence infrastructure