Group 2

2.2 A Layout-aware Methodology for Path-delay Fault Grading and Diagnosis, Pis: S. Tragoudas, T. Haniotakis, SIUC

Center for Embedded Systems
An NSF Industry/University Cooperative Research Center

A Layout-Aware Methodology for Path-Delay Fault Grading and Diagnosis

Spyros Tragoudas, SIUC
Themistoklis Haniotakis, SIUC

SIU Southern Illinois University CARBONDALE

NATIONAL SCIENCE FOUNDATION

ASU Ira A. Fulton Schools of Engineering ARIZONA STATE UNIVERSITY

Project Overview and Description

Challenges

- Continued scaling of devices has resulted in
  - Various abnormalities in IC behavior
  - Signal integrity issues
- Accounting for such variations during ATPG greatly increases its complexity
- Quality of test set should be based on
  - The timing behavior of the covered paths
  - The coverage of process and environmental variations affecting timing in given IC

Proposed Solution

- Implicit layout-aware grading of path-delay faults.
- Characterizing path criticalities based on layout information.
- Diagnosis of faults sensitive to a target parameter.

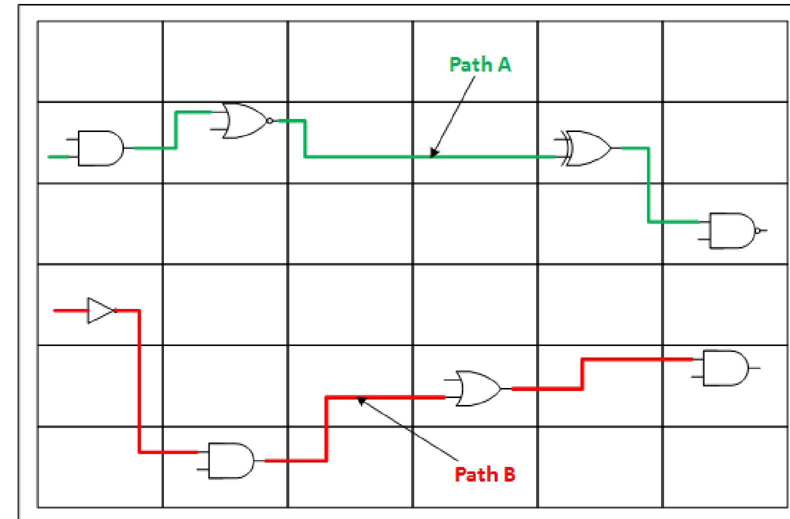
Approach

Layout information is available as

- **Design Exchange Format (DEF)**
  - Contains physical placement information of elements in the circuit
- **Library Exchange Format (LEF)**
  - Contains the information on the various parameters of the elements in the circuit

Build a ZBDD of paths sensitized by the given test set

Information from above DEF and LEF files is annotated with each node in the ZBDD



Two timing critical paths A and B

$D(A) \approx D(B)$

ρ_i^A = Sensitivity of path A to parameter i.

ρ_i^B = Sensitivity of path B to parameter i

If ($\rho_i^A > \rho_i^B$) then

w.r.t i

prob(A > clk) > prob(B>clk)

i.e. Path A is more critical than path B

Novelty

Fault Grading

Traditionally: Obtain coverage as the number of timing critical paths sensitized by the given test set

Proposed: Obtain coverage based not only on timing behavior but also, the processes covered by the paths

This gives way to define new metrics for test quality and more precise estimation of DPM

Diagnosis

- Diagnosis of defects due to manufacturing variations has always been a daunting task
- With the proposed approach one a quickly grab the set of all paths affected by a given variation
- Diagnosis can then easily proceed to locate the affected site in the layout

Project Tasks/ Deliverables

	Description	Date	Status
1	Software tool to perform layout-aware path grading and thereby, estimate test set quality.	Jan-2015	*Partially complete* *(to be built on existing tools at SIUC)*
2	Software tool to aid failure analysis using layout information.	Aug-2015	*Not yet started*

Executive Summary

Benefits

1. A layout-aware path grading tool.
2. A new layout-aware metric for calculating test set quality.
3. A tool for effective failure analysis by leveraging layout information.

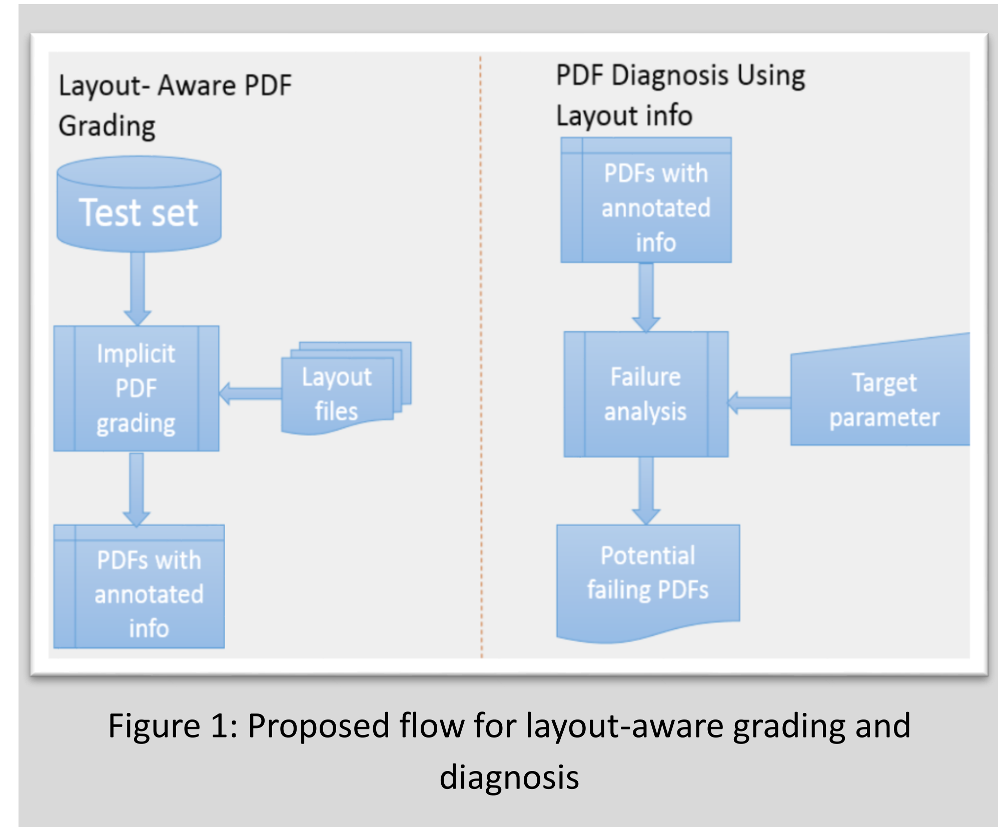


Figure 1: Proposed flow for layout-aware grading and diagnosis