Group 2

2.4 Comparison of Image Processing Algorithms on Micro-array Architectures and GPGPU Platforms, PI: S. Tragoudas, SIUC

Center for Embedded Systems

An NSF Industry/University Cooperative Research Center

Comparison of Image Processing on Micro-Array Architectures and GPGPU Platforms

Dr. Tragoudas, SIU

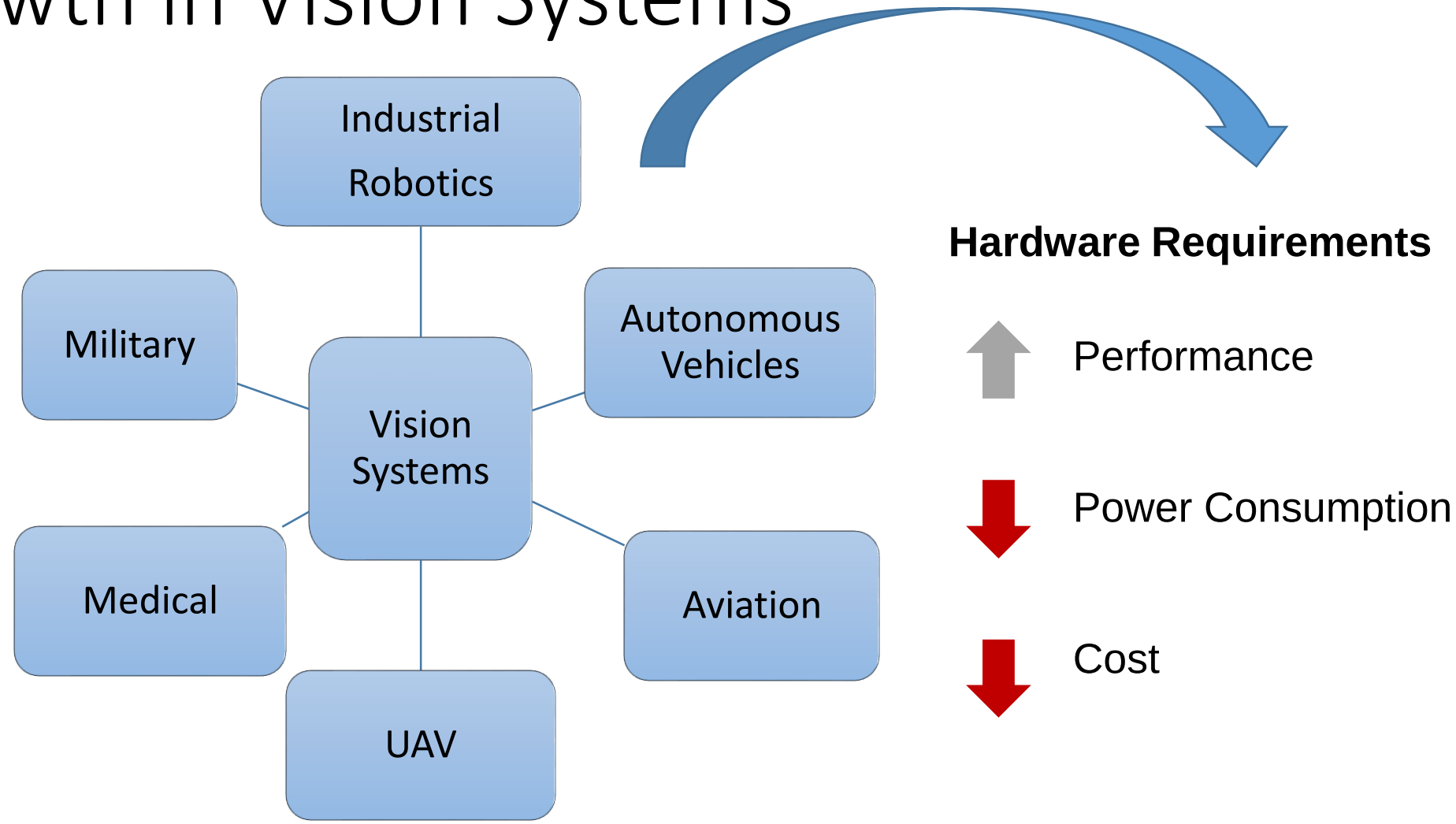
Luke Pierce, Daniel Olsen, Garret Kaiser

SIU Southern Illinois University CARBONDALE

National Science Foundation

ASU Ira A. Fulton Schools of Engineering ARIZONA STATE UNIVERSITY

Growth in Vision Systems



Project Overview and Description

- Comparison of GPGPU vs Micro-Array general CPUs Solutions
  - Quantify speed, power, and cost tradeoffs
- Explore solution space of existing image processing algorithms for targeted platforms
  - Power vs Performance

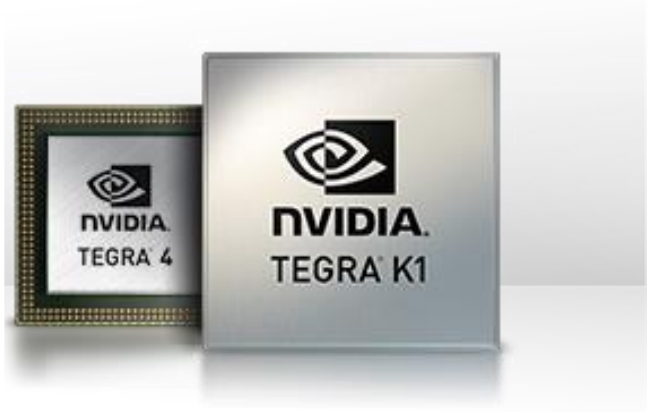
Selection of GPU

High Performance GPGPU Option

Workstation GPU
CUDA/OpenCL
State of the Art

Embedded Low Power GPGPU Option

Tregra TK1
- **192 Cores**
- **First Mobile CUDA Platform**
- **28nm Process**



Optimization of Image Processing

- Several image processing algorithms will be selected
  - Noise Reduction
  - Image Transforms
- Algorithms will be optimized for platform
  - CUDA/OpenCL
  - Micro Array
- Algorithms will benchmark platforms to determine performance

Project Tasks/ Deliverables

	Description	Date
1	Select GPGPU Platforms	8/31/2014
2	Select Image processing algorithms	9/30/2014
3	Implement and optimize image processing algorithms on GPGPU platforms	12/20/2014
4	Port algorithms to micro-array system	3/31/2015
5	Generate final report detailing the performance results and trade-offs for each platform	7/31/2015

Executive Summary

- Analyze trade-offs of current gen. GPGPUs vs Multi-Core CPUs
  - Emphasis on the embedded domain
  - Include state of the art low power GPGPU technology

- Optimization of Image Processing algorithms for GPGPU Technology
  - Noise Removal Algorithms
  - Data Parallelizable
  - Scalability