Center for Embedded Systems

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Towards Predictable Execution of Safety-Critical Tasks on Mixed-Criticality Multi-Core Platforms.

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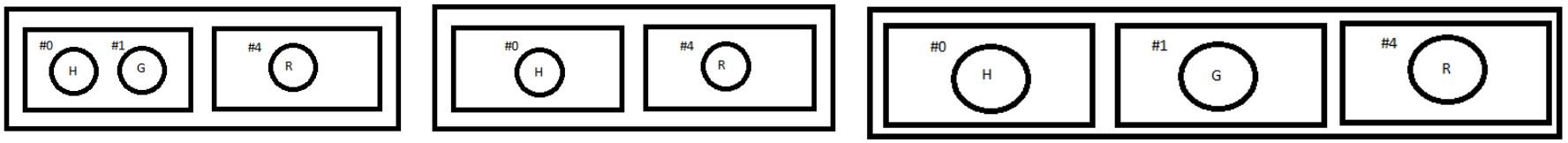
Project Overview and Description

- **Project Description**
  - Integrate independent High-Safety Sensitive (HSS) and Low-Safety Sensitive (LSS) applications onto one physical computing platform
  - Characterize HSS behavior in presence of LSS tasks
  - Develop policies to execute HSS applications in a deterministic fashion
- **Problem**
  - Deterministic predictable execution of HSS in the presence of LSS tasks
- **Feasible Solution**
  - Use modern virtualization (hypervisor) technology to isolate HSS and LSS application on a multi-core platform
  - Use shared resource isolation for HSS tasks for predictable execution times
- **Applications**
  - Integrate multiple avionics modules in a “single box”
  - Investigation on Freescale P4080 paltform

Approach

Configurations

- **Agents:** Hypervisor (H) General Purpose System(GP) Real-time System (RT)
- **Partitions :**



- **L3 Cache:** 32 ways

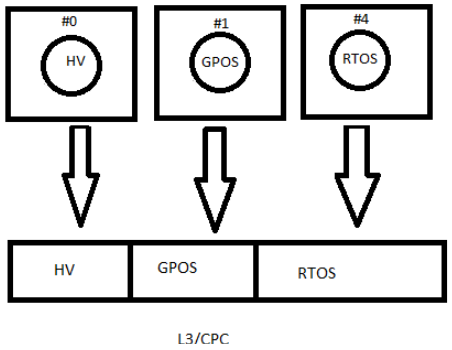
32	0
24	8
16	16
8	24
0	32

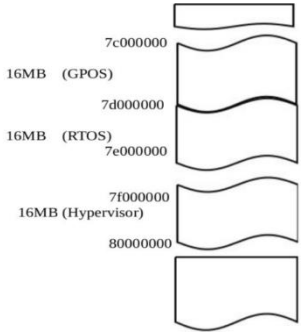
0	0	32
4	0	28
8	0	24
16	0	16
32	0	0
6	4	22
8	4	20
12	6	14

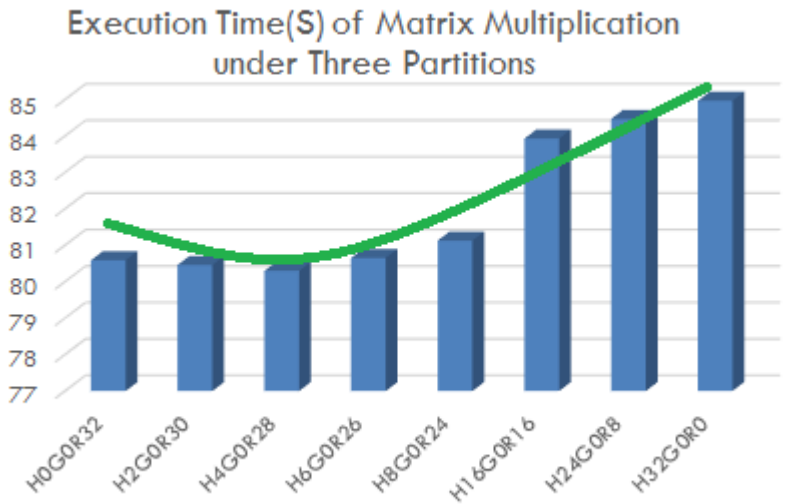
- **Workloads:** Matrix Multiplication, Random Memory Reads, Sorting.

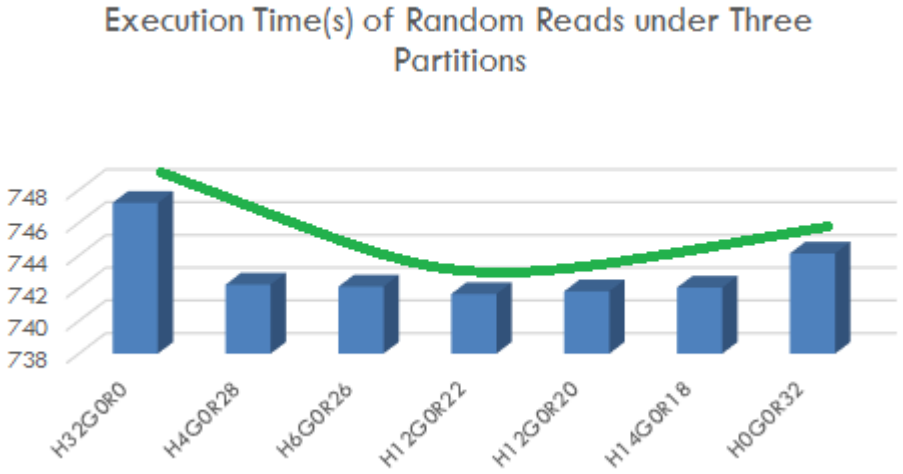
Project Status

- Isolation of Physical Memory Area (PMA) for each partitions.
- Examined the effect on RT under different configuration of partitions/L3 Cache.
- Studied the effect of the Hypervisor overhead and identified the “Bell Effect”.







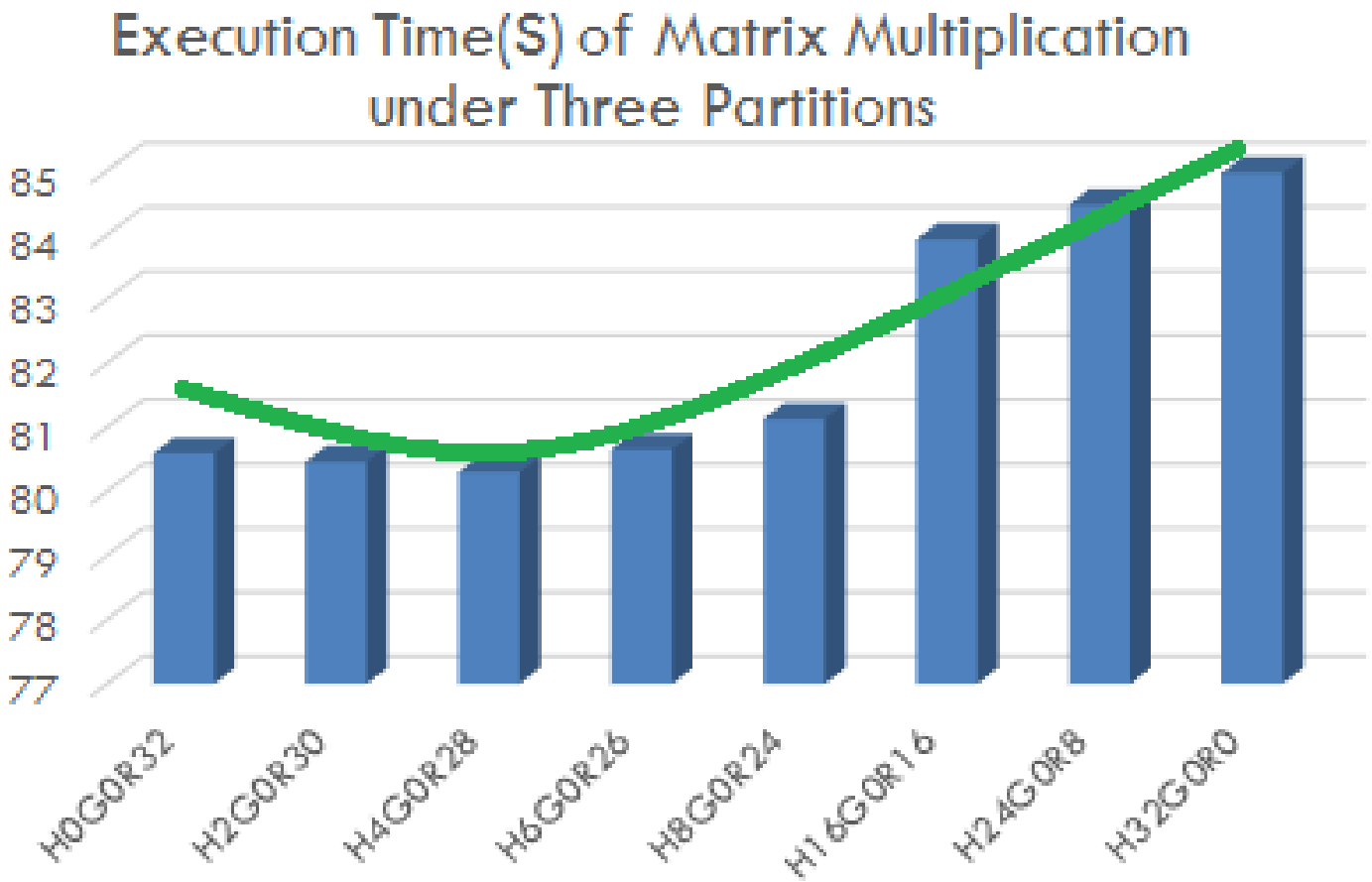


Project Tasks/ Deliverables

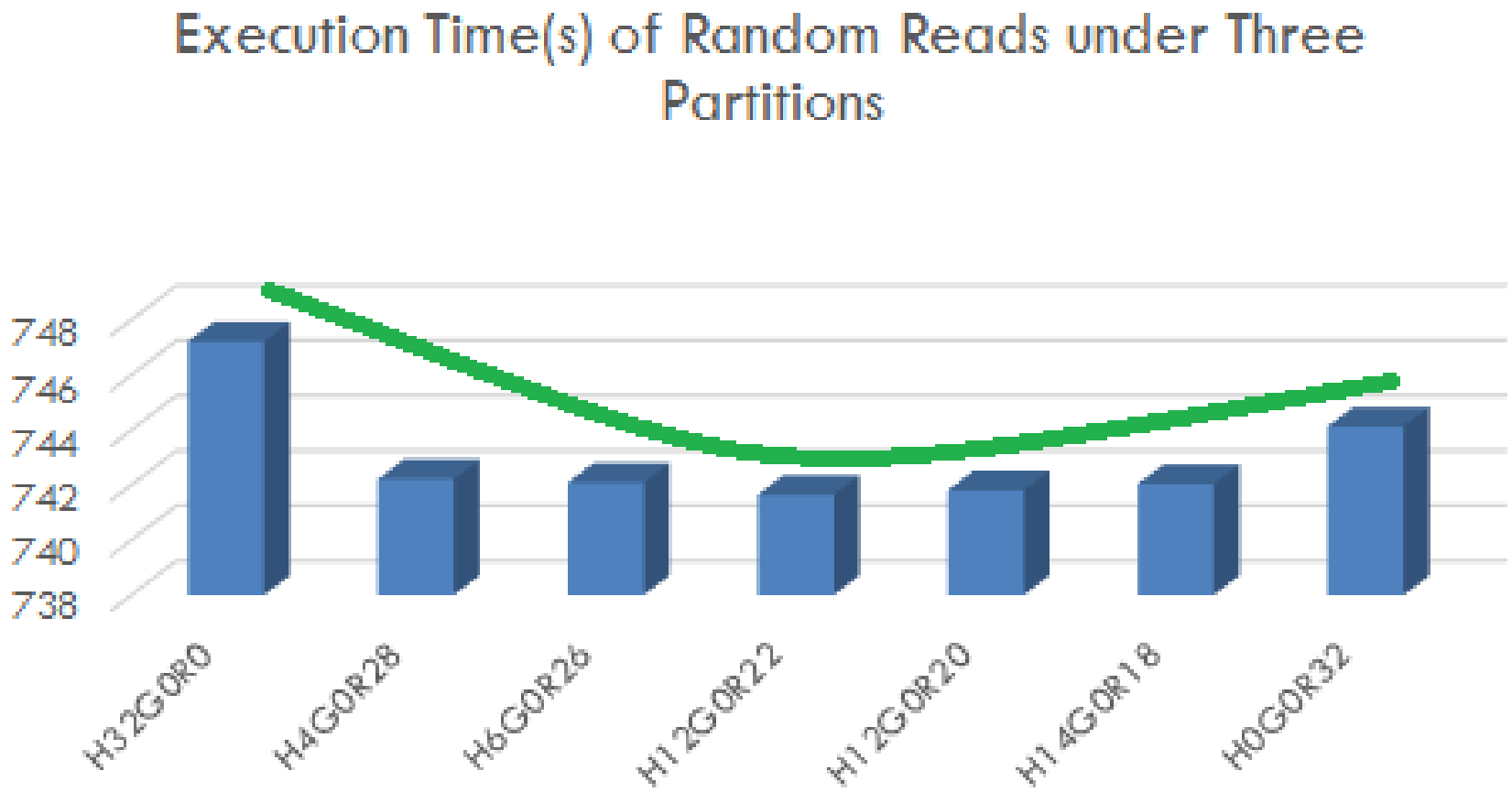
	Description	Date	Status
1	Isolation of Physical Memory Area (PMA) for Hypervisor, GPOS and RTOS.	Fall 14	
2	Extensive Experimentation with multidimensional configurations.	Fall 14	
3	Identification of the Bell shaped behavior.	Fall 14	
4	Additional Experimentation on configurations (multiple dimensions).	Spring 15	
5	Effects of Memory-Intensive and Processor-intensive GP applications on the RT side.	Spring 15	
6	Effect of Number of cores assigned to each partition.	Spring 15	

Bell Effect

The Hypervisor needs a sufficient amount of cache for the RT to run at its best.

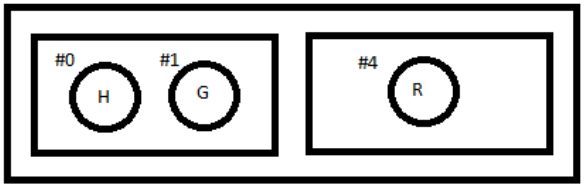


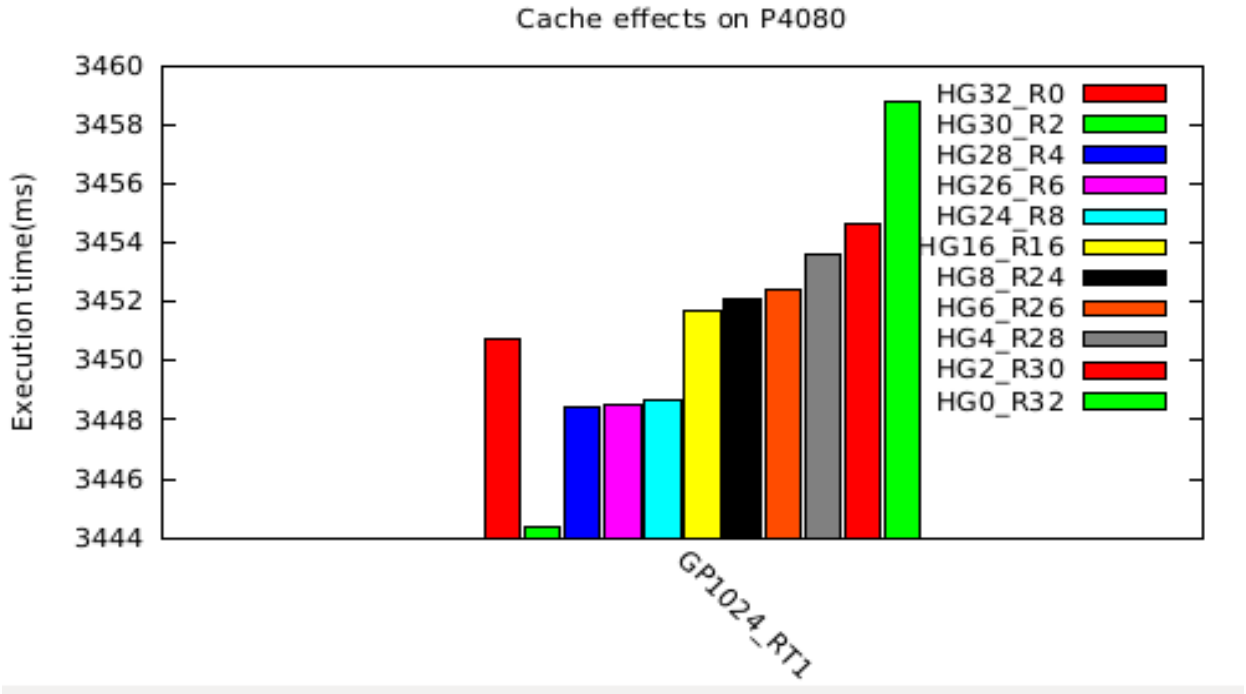
Bell Effect 2



Effect of shared Bus Bandwidth

GP: Stride_1024; RT : Stride_1
(Two Partitions)

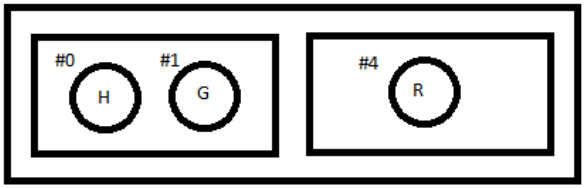


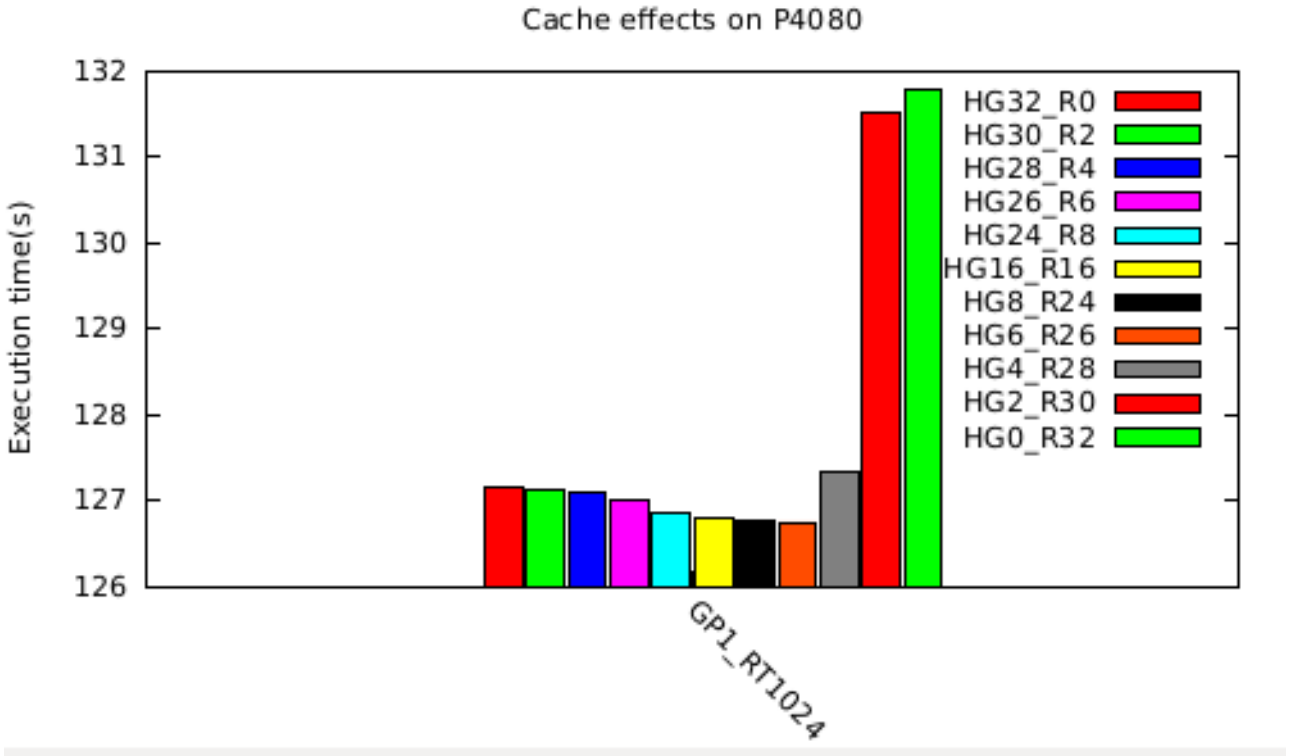


Best: HG30_R2

Effect of shared Bus Bandwidth

GP: Stride_1;RT : Stride_1024
(Two Partitions)

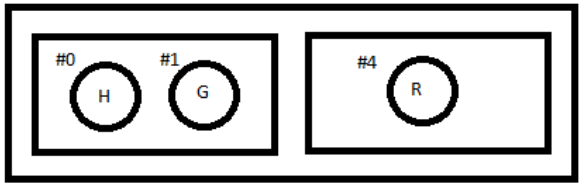


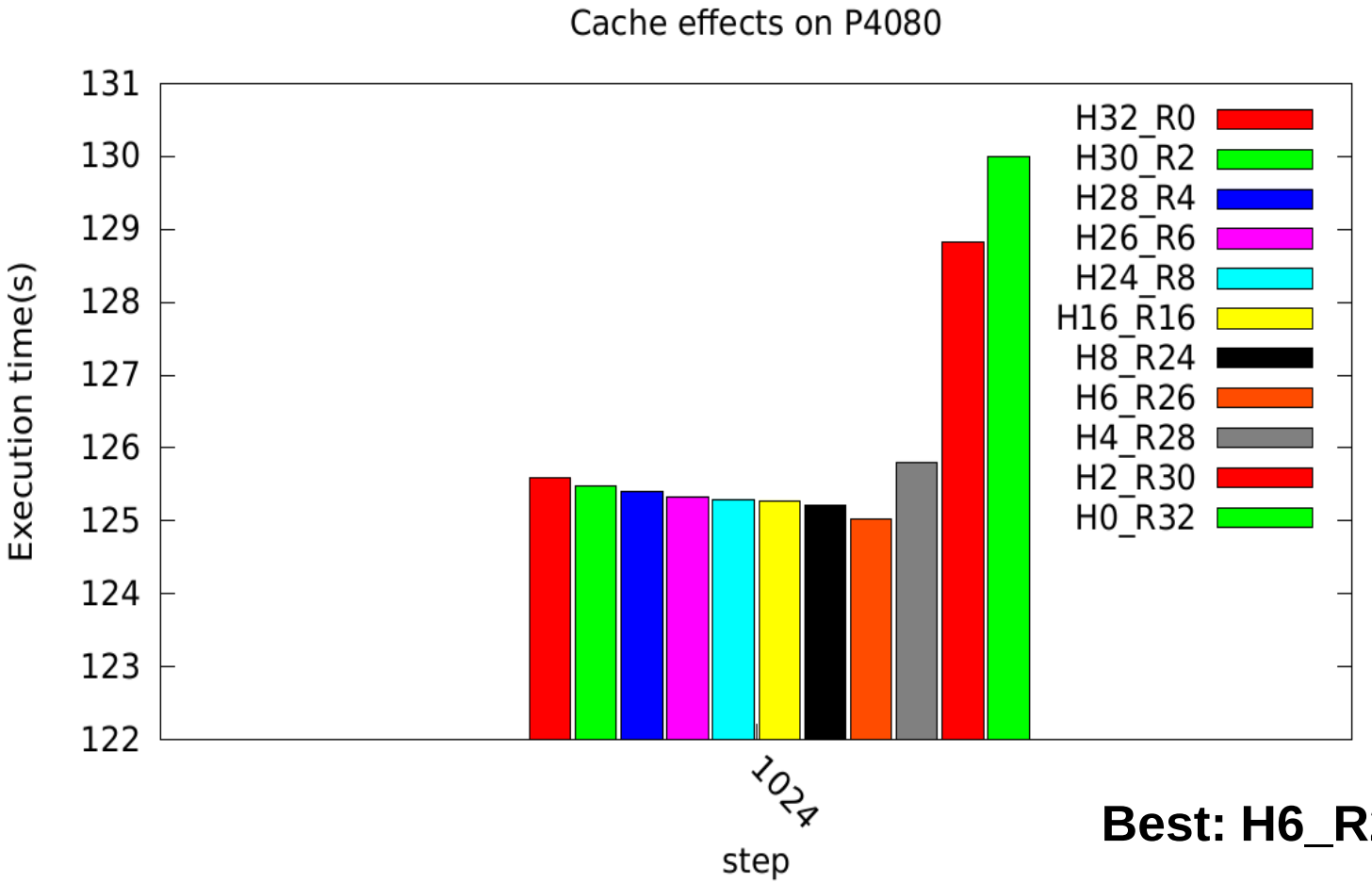


Best: HG6_R26
H needs 4 !

Effect of number of partitions on Hypervisor overhead

Two Partitions
GP: No program ; RT: Stride_1024

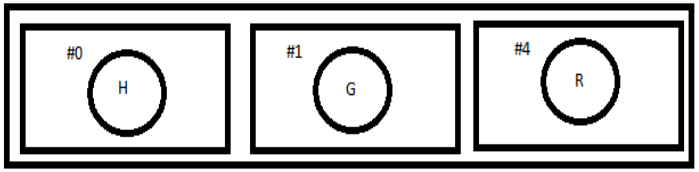


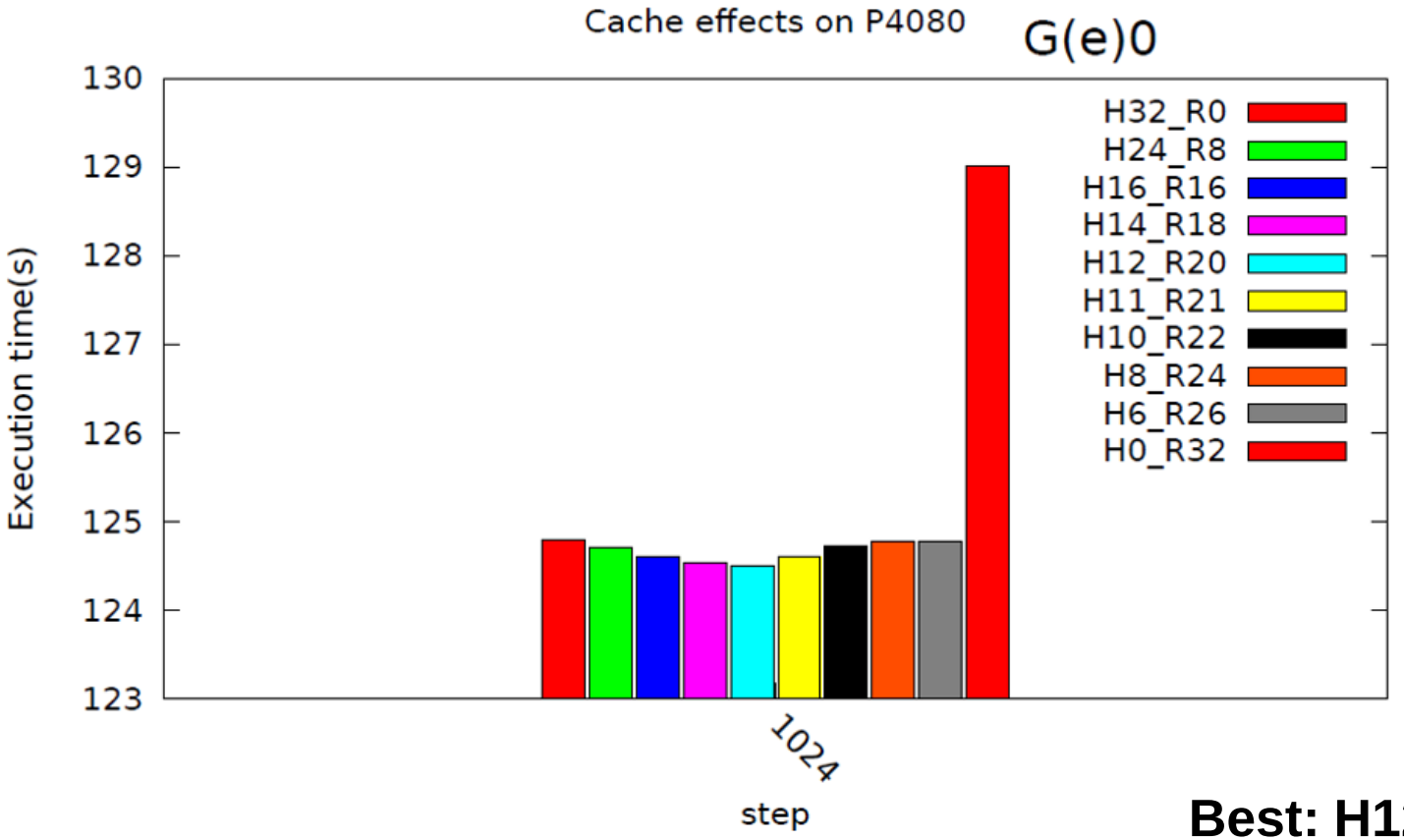


Best: H6_R26

Effect of number of partitions on Hypervisor overhead

Three Partitions
GP: No program ; RT: Stride_1024





Best: H12_R20