Center for Embedded Systems

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A Layout-Aware Methodology for Path-Delay Fault Grading and Diagnosis

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Project Overview and Description

Challenges

- Continued scaling of devices has resulted in
  - Various abnormalities in IC behavior
  - Signal integrity issues
- Accounting for such variations during ATPG greatly increases its complexity
- Quality of test set should be based on
  - The timing behavior of the covered paths
  - The coverage of process and environmental variations affecting timing in given IC

Proposed Solution

- Implicit layout-aware grading of path-delay faults.
- Characterizing path criticalities based on layout information.
- Diagnosis of faults sensitive to a target parameter.

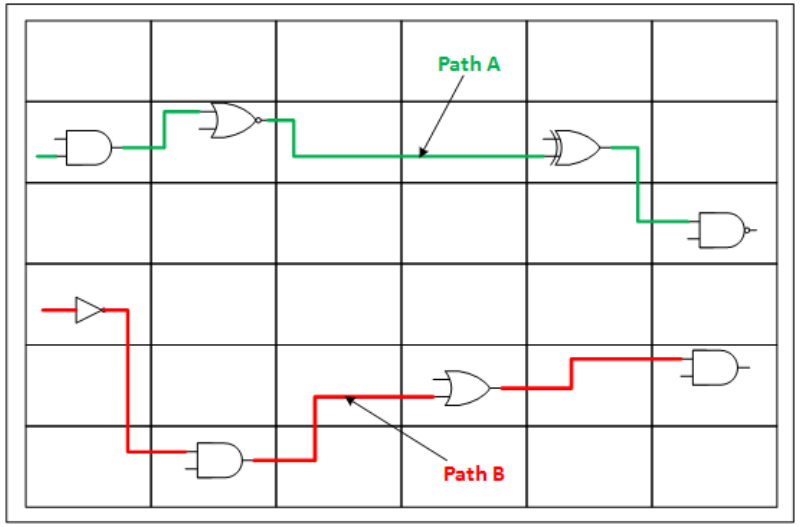
Approach

Layout information is available as

- **Design Exchange Format (DEF)**
  - Contains physical placement information of elements in the circuit
- **Library Exchange Format (LEF)**
  - Contains the information on the various parameters of the elements in the circuit

Build a ZBDD of paths sensitized by the given test set

Information from above DEF and LEF files is annotated with each node in the ZBDD



Two timing critical paths A and B

$D(A) \approx D(B)$

ρ_i^A = Sensitivity of path A to parameter i.

ρ_i^B = Sensitivity of path B to parameter i

If $(\rho_i^A > \rho_i^B)$ then

w.r.t i

prob(A > clk) > prob(B>clk)

i.e. Path A is more critical than path B

Novelty

Fault Grading

Traditionally: Obtain coverage as the number of timing critical paths sensitized by the given test set

Proposed: Obtain coverage based not only on timing behavior but also, the processes covered by the paths

This gives way to define new metrics for test quality and more precise estimation of DPM

Diagnosis

- Diagnosis of defects due to manufacturing variations has always been a daunting task
- With the proposed approach one a quickly grab the set of all paths affected by a given variation
- Diagnosis can then easily proceed to locate the affected site in the layout

Benefits to industry

Benefits

1. A layout-aware path grading tool.
2. A new layout-aware metric for calculating test set quality.
3. A tool for effective failure analysis by leveraging layout information.

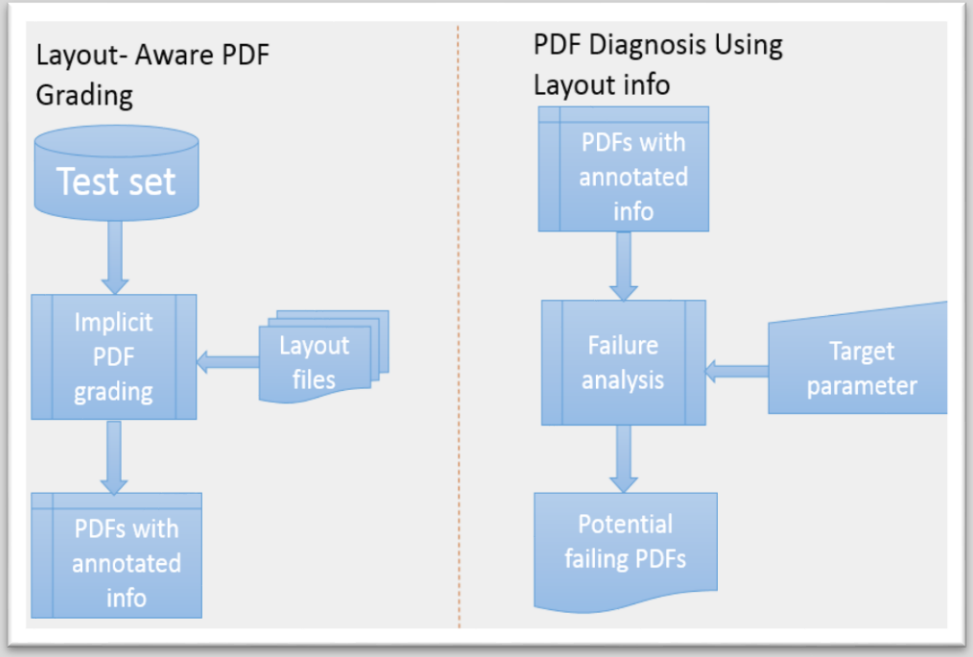


Figure 1: Proposed flow for layout-aware grading and diagnosis

Project Status

DEF parser

- Position of individual cells
- Statistics on interconnect lengths, metal layers, vias etc..
- Power distribution network (power rings, power straps and rails)

Coupling Report

- Identify aggressor nets for interconnects along sensitized paths

Layout and process variations aware models for

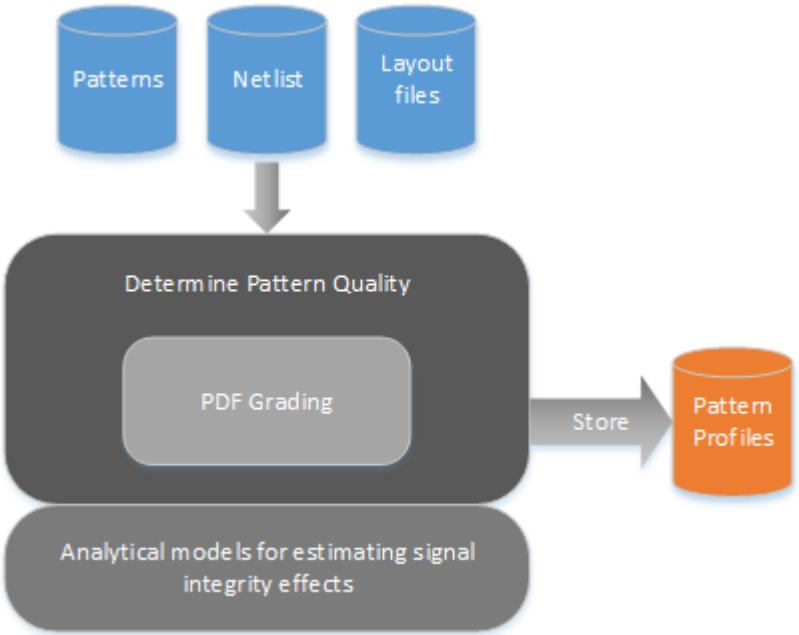
- Precisely capturing the effect of crosstalk on path delays
- Measuring pattern's quality in exciting delay degrading crosstalk effects along the sensitized paths
- Creating a pattern profile to aid future defect diagnosis

Project Tasks/ Deliverables

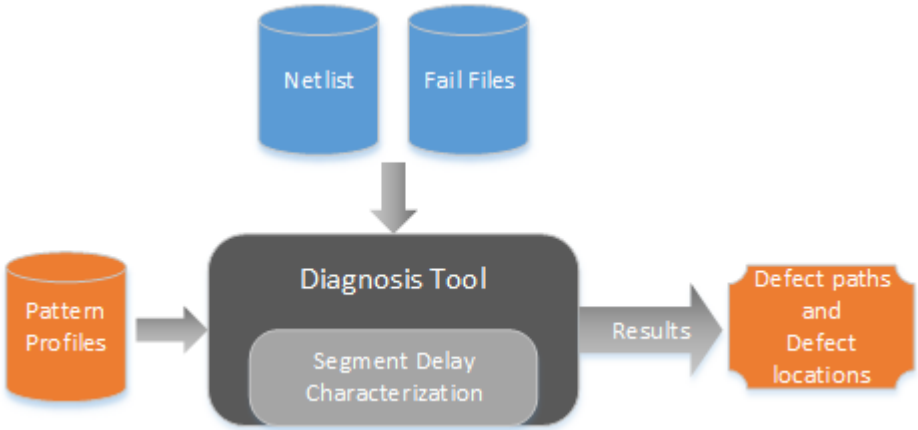
	Description	Date	Status
1	DEF parser to extract layout information	Jan-2015	*Complete*
2	Tool to annotate ZBDD nodes with layout characteristics/statistics of corresponding circuit elements	Jan-2015	*Complete*
3	Tool to evaluate pattern quality and create pattern profile	Aug-2015	*Partially Complete*
4	Software tool to aid failure analysis using layout information.	Aug-2015	*Not yet started*

Executive Summary

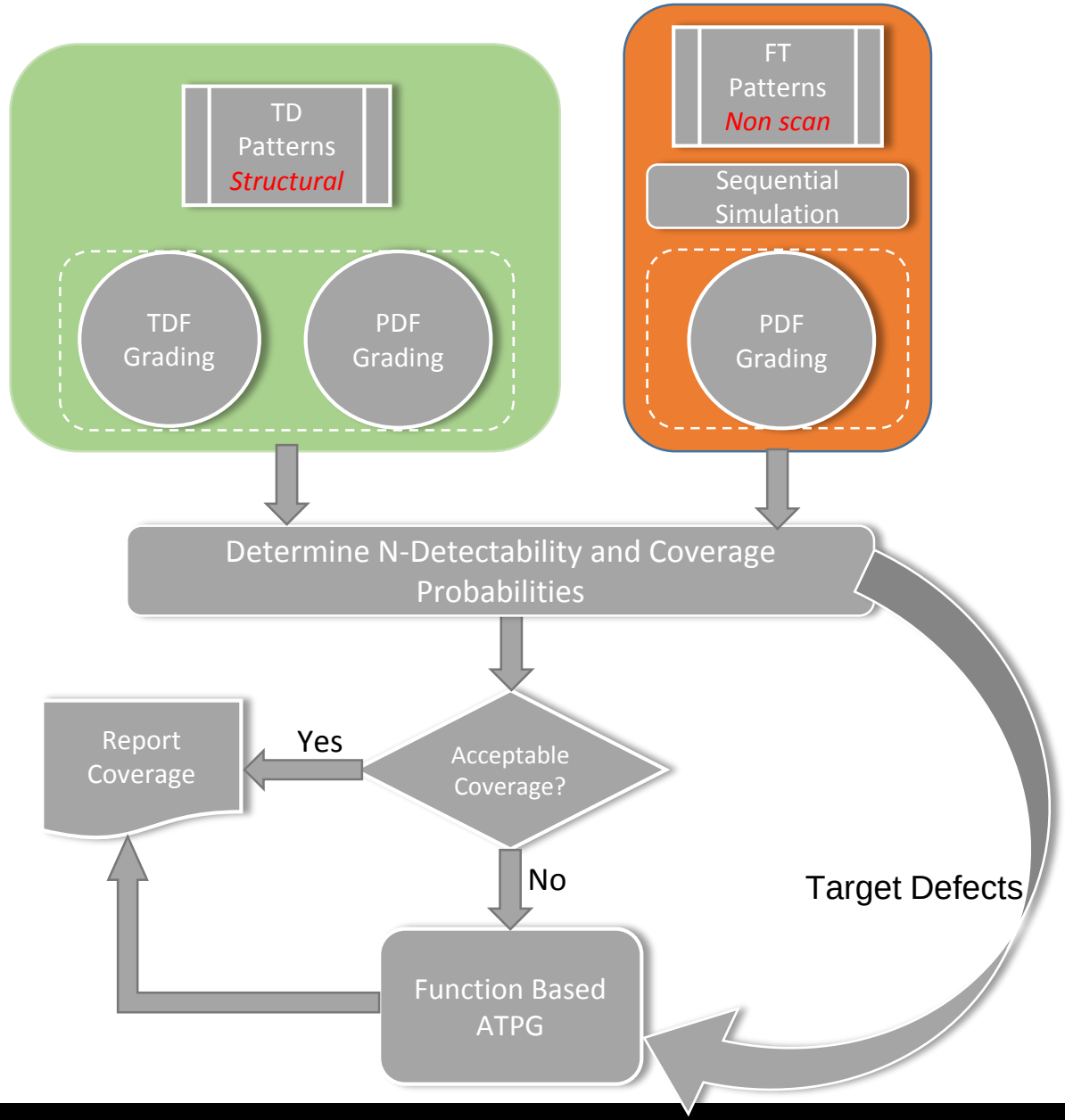
Phase 1- Layout aware pattern quality analysis



Phase 2- Layout aware diagnosis of defective paths and segments



Previous work – Year 4



Related work in literature

- The authors in [4] and [5] deal with layout-aware pattern grading
- [4] presents a test pattern generation method that would generate a pattern to excite the longest delay by introducing crosstalk and power supply noise effects
- [5] characterizes the different patterns available for a path based on their ability to produce crosstalk and power supply noise effects
- The intensions of the authors in [4] and [5] was to generate test patterns considering signal integrity effects only and therefore, provide little assistance towards diagnosing potential faults using layout information.

Pattern dependent defects

- Aggressors of victims along sensitized paths are identified using layout files and coupling report
- The type of transition along aggressors determine the speed up or slow down along victim lines
- The skew between aggressor and victim lines determines the amount of speed up or slowdown along victim lines

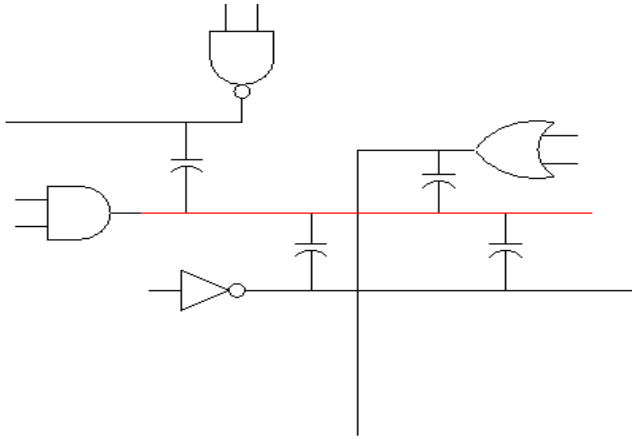
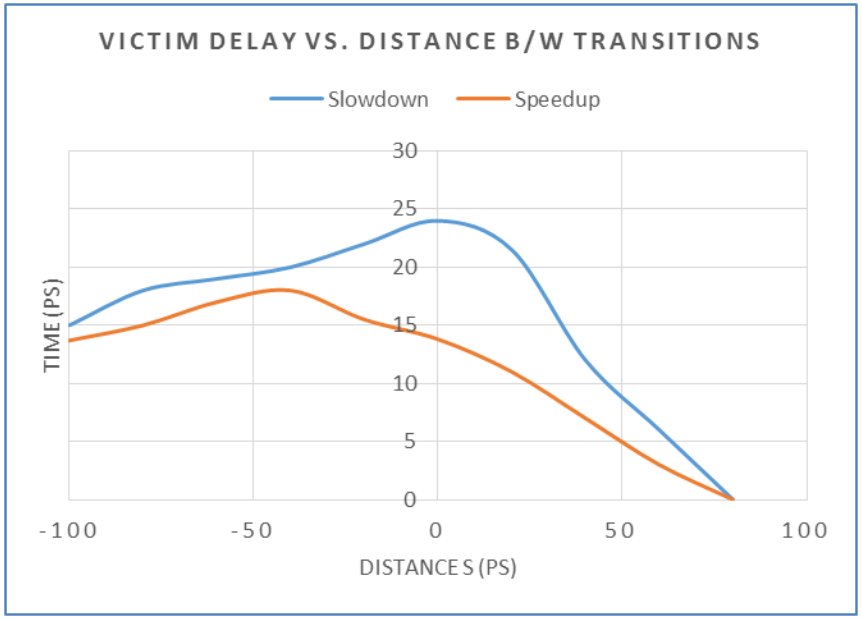


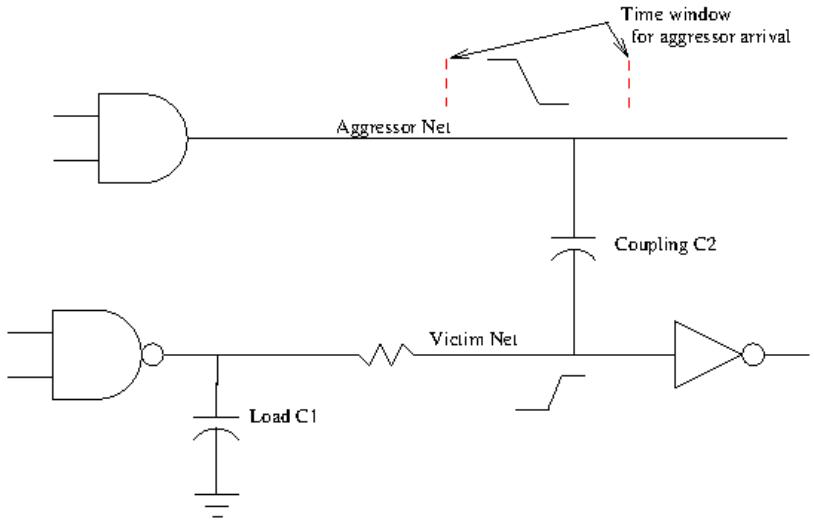
Figure 4- Crosstalk victim and aggressors



Capturing Crosstalk Effects

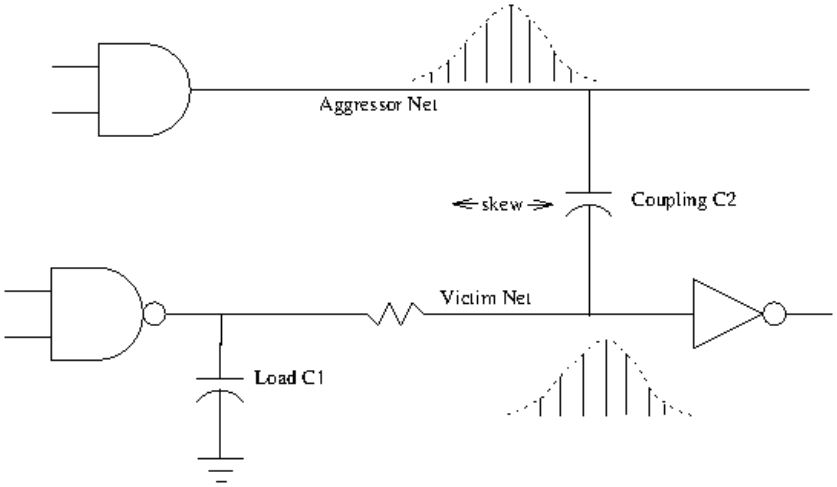
Traditional Crosstalk analysis

- Assumes simultaneous switching
- Assumes max delay due to crosstalk excitation

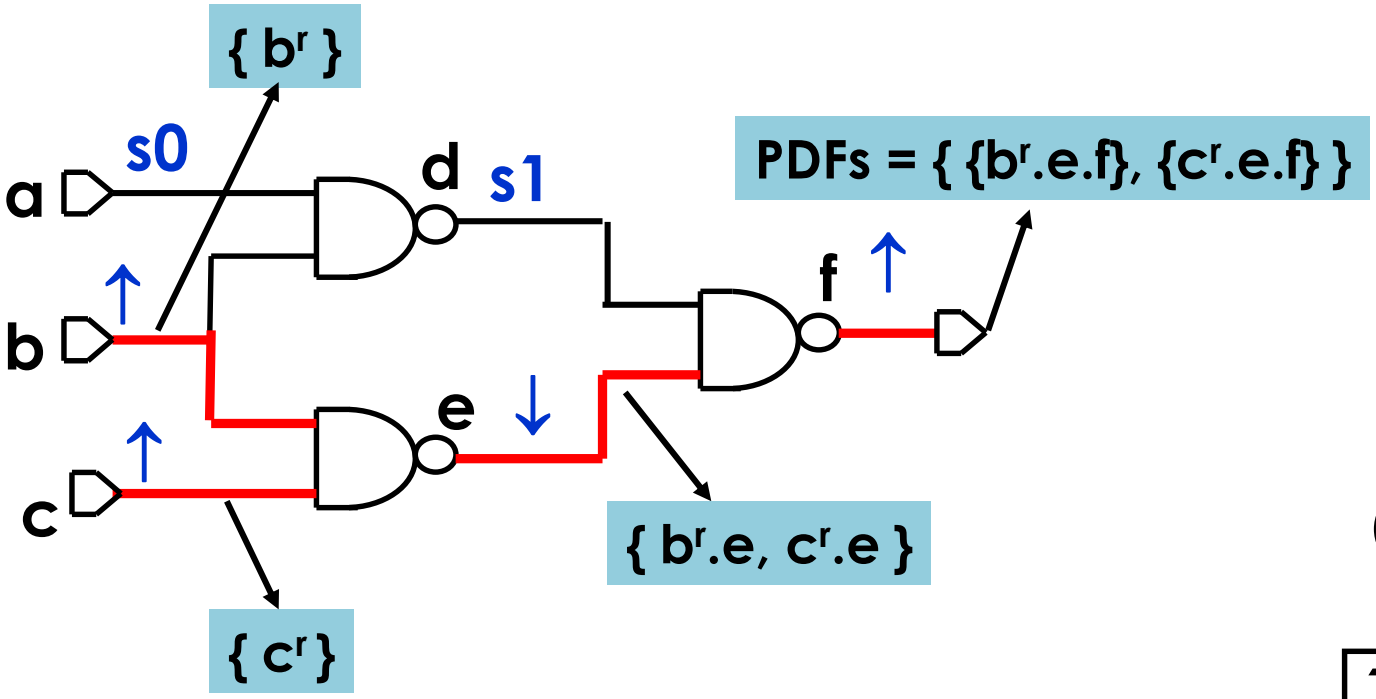


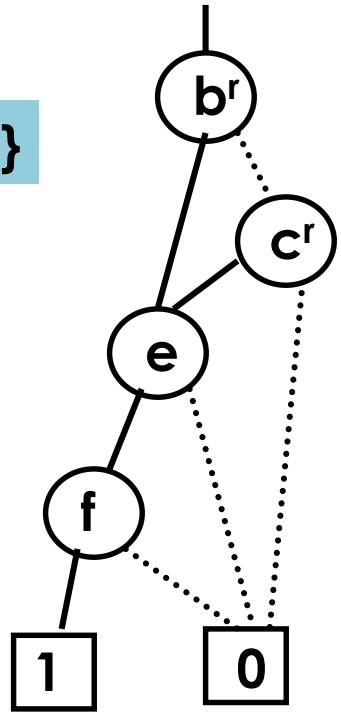
Proposed Crosstalk analysis

- Consider statistical arrival times to account for process variations
- Consider skew b/w transitions to calculate coupling effect
- Propagate effected delays from PI to PO



PDF grading using ZBDDs



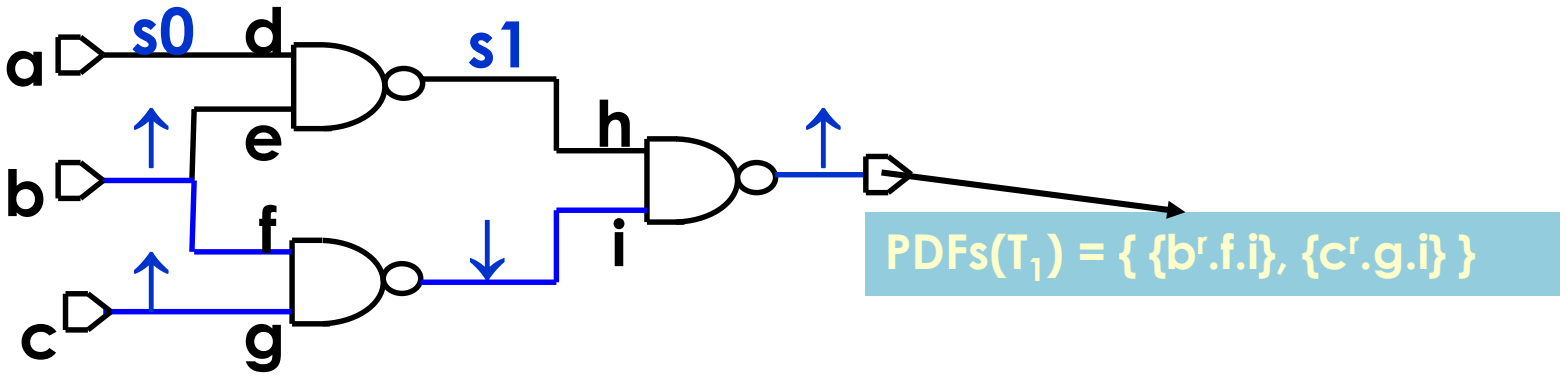


Full-scan PDF Grading

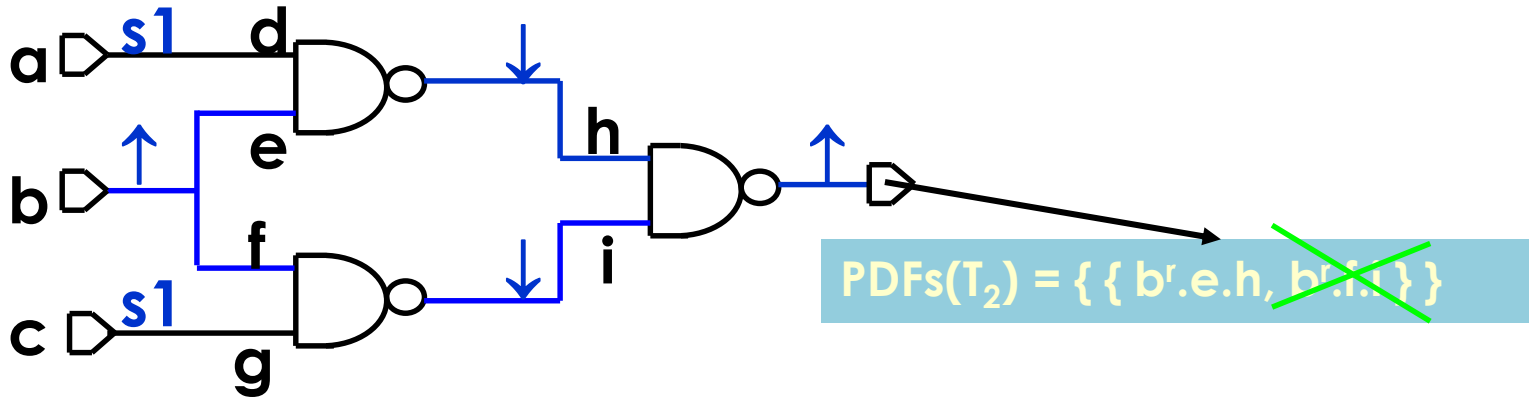
ZBDD

Implicit Grading for PDFs

Simulate & store PDFs for T_1 = {000, 011}



Simulate & store PDFs for T_2 = {101, 111}



Faults Covered (T) = PDFs(T1) ∪ PDFs(T2)

Eliminate redundant faults

References

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