Center for Embedded Systems
An NSF Industry/University Cooperative Research Center

Year 6: Industry Advisory Board (IAB) Mid-term Update Meeting
February 3-4, 2015
Arizona State University

AGENDA
Revised: January 30, 2015, v6

Objectives

- Provide a forum for NSF, IAB members, faculty, students, and guests to interact and discuss research projects, areas of interest, and opportunities
- Deliver a brief update on Center activities, mid-term update on Year 6 projects
- Conduct IAB business meeting

Tuesday, February 3, 2015

7:30 - 8:00 am	**Registration Check-in and Coffee, ASU campus, Old Main,** 400 E. Tyler Mall, Tempe, AZ 85281 (south of University Dr., just east of College Ave.)
8:00 – 8:15 am	**Welcome,** Sarma Vrudhula, Director, Center for Embedded Systems **Introductions**, Sarma Vrudhula (ASU), Spyros Tragoudas, Site Director SIU
8:15 – 8:30 am	**NSF Message,** Craig Scott, University of Washington, NSF Evaluator
8:30 – 9:30 am	**Keynote Address / Q&A Session:** Dr. Vivek K. De, Intel Fellow & director of Circuit Technology Research, "Energy Efficient Computing in Nanoscale CMOS: Challenges and Opportunities"
9:30 – 9:40 pm	**BREAK**
9:40 – 9:45 am	**Presentation Format Overview,** Rathish Jayabharathi, Intel Corporation, CES – IAB chair
9:45 – 10:15 am (5 min presentations)	**Industry Presentations:** 1. UTC Aerospace Systems 2. Intel 3. Toyota 4. Marvell 5. Qualcomm 6. Johnson Controls
10:15 – 11:15 am	**Industry Poster Session**
11:15 – 12:10 pm	**LUNCH**
12:10 – 12:35 pm (3 min presentations)	**Mid-term Research Updates**, year 6 projects – GROUP 1 1.1 Parallelization of Embedded Control Applications on Multi-core Architectures: A Case Study, Georgios Fainekos, Yann-Hang Lee (ASU), A1.Y6.GF.YHL 1.2 Comparison of Image Processing Algorithms on Micro-array Architectures and GPGPU Platforms, Spyros Tragoudas (SIU), S3.Y6.ST 1.3 Performance Optimal Control of a System of Interconnected Components Under Thermal and Energy Constraints (YEAR II), Sarma Vrudhula (ASU), A4.Y6.SV 1.4 Cortical Processor based RRAM, Shimeng Yu (ASU), *A10.Y5.SY 1.5 Design of Ultra-low Power Circuits for Compressive Sensing in Mobile Devices, Sarma Vrudhula, Yu (Kevin) Cao (ASU), A3.Y6.SV.YC 1.6 Towards Predictable Execution of Safety-Critical Tasks on Mixed-Criticality Multi-Core Platforms, Dimitrios Kagaris (SIU), S1.Y6.DK 1.7 Optimized Switching Pattern Generator Embedded into an SoC, Constantine Hatziadoniu (SIU), S5.Y6.CH

12:35 – 1:55 pm	**Poster Session**, year 6 projects – GROUP 1
1:55 – 2:15 pm	**Complete LIFE Forms online (10 minutes)**, year 6 projects – GROUP 1 **LIFE Forms Feedback: Discussion (10 minutes)**, year 6 projects – GROUP 1
2:15 – 2:40pm (5 min presentations)	Industry Guest Presentations: 1. Robert Bosch GmbH, Rainer Gmehlich 2. Advanced Micro Devices, Timour Paltashev 3. The Boeing Company, Russell Enns Academic Site Presentations: 1. University of Virginia, Dr. Mircea Stan 2. University of Oregon, Dr. Michel Kinsy
2:40 – 3:05 pm (3 min presentations)	**Mid-term Research Updates**, year 6 projects – GROUP 2 2.1 Energy-aware Application Scheduling for Heterogeneous and Parallel Smart Phone Architectures, Carole-Jean Wu (ASU), A2.Y6.CW 2.2 Automated Testing for Functional Coverage for Cyber-Physical Systems, Georgios Fainekos (ASU), A5.Y6.GF 2.3 Synchronizing Finite State Machine Controllers for Distribution Systems. Dimitrios Kagaris (SIU), S4.Y6.DK.DIST 2.4 A Layout-aware Methodology for Path-delay Fault Grading and Diagnosis, Spyros Tragoudas, Themistoklis Haniotakis (SIU), S2.Y6.ST.TH 2.5 Background Invariant Laser-spot Detection and Tracking for Embedded Systems, Lalit Gupta (SIU), S6.Y6.LG 2.6 I2AV: Integrate, Index, Analyze, and Visualize Energy Data for Data-driven Simulations and Optimizations, K. Selcuk Candan (ASU), *A9.Y5.KSC 2.7 Testability and Timing Analysis in Nanoscale Designs in the Presence of Process Variations, Spyros Tragoudas (SIU), Sarma Vrudhula (ASU), Themistoklis Haniotakis (SIU), Fundamental Research Project, Y6.ST.SV.TH.FRP.Nano Poster Only: Low Voltage, Low Power and Robust Threshold Logic Gate with RRAM Devices (*formerly Spintronic Threshold Logic Array*), Sarma Vrudhula (ASU), *A6.Y5.SV.SPIN
3:05 – 4:25 pm	**Poster Session**, year 6 projects – GROUP 2
4:25 – 4:45 pm	**Complete LIFE Forms online (10 minutes)**, year 6 projects – GROUP 2 **LIFE Forms Feedback: Discussion (10 minutes)**, year 6 projects – GROUP 2
4:45 – 5 pm	**State of the Center,** Sarma Vrudhula, Director, Center for Embedded Systems
6:00 pm	**Happy Hour & Dinner (all),** Rúla Búla Irish Pub, 401 S. Mill Ave.

<u>Wednesday, February 4, 2015</u>

8 – 10:30 am	**Light Breakfast, IAB meeting (closed session), ASU's Centerpoint Bldg,** 660 S. Mill Ave., 2nd Floor, conference room 203-03