Center for Embedded Systems (CES)
Request for Proposals Template – YEAR 6

DUE: Monday, March 31, 2014, by 5 p.m.

TITLE:	**Towards Predictable Execution of Safety-Critical Tasks on Mixed-Criticality Multi-Core Platforms.**				
PI:	Dimitri Kagaris Harini Ramaprasad	**EMAIL:**	kagaris@engr.siu.edu harinir@siu.edu	**TEL:**	618-453-7973 618-453-4755
DEPT:	Electrical and Computer Engineering	**SCHOOL:**	Southern Illinois University Carbondale		

ABSTRACT: (250 OR FEWER WORDS)

Multi-core architectures are a natural choice for integrating multiple independent functionalities into a single node in a cost- and space-effective manner. However, for systems with multiple levels of criticality, transporting highly safety-sensitive (HSS) applications (such as those for avionics systems with Design Assurance Level (DAL) of grade from DAL-C to DAL-A) onto a multi-core platform and sharing the benefits of the new computing environment with other less safety-sensitive (LSS) applications that have lower assurance levels but may be computation-intensive presents challenging problems in ensuring predictability/determinism of the HSS applications while still maintaining acceptable Quality of Service (QoS) for the LSS applications. The dominant approach towards isolating HSS and LSS tasks is the use of a virtualization environment (hypervisor) on top of the underlying multi-core platform. In prior work, extensive experimentation was conducted on the Freescale P4080 platform to characterize the behavior of HSS tasks in the presence of LSS tasks when executing them on different, statically derived partitions residing on separate cores. The goals of the proposed project are to apply the results of this characterization to end-use scenarios and to develop policies to exploit hardware mechanisms such as cache locking, cache partitioning and message passing among partitions to maintain determinism of HSS applications under regular and overload situations while maintaining QoS for the LSS applications.

PROBLEM:

Deterministic execution of HSS tasks in the presence of LSS tasks and other HSS tasks is challenging. The goal of this project is to develop and compare policies to maintain responsiveness of HSS applications under regular and overload situations.

RATIONALE:

The results of the proposed study will be instrumental in enabling safe deployment of mixed-criticality tasks on multi-core processors with support for virtualization.

APPROACH:

The PIs propose to employ the following approach to achieve the goals of the proposed project:

1. Cache locking and partitioning are effective techniques to improve the predictability of HSS tasks and several policies for the same have been proposed. The PIs propose to explore the application of specific policies such as *minimize utilization* (Lock-MU) and *minimize interferences* (Lock-MI) [13] to end-use scenarios, identified by the workload characterization conducted in prior work.

2. Hypervisors typically allow configuration of one partition as a manager, giving this partition rights to pause and resume other partitions. The PIs propose to explore the use of such a manager partition a) to dynamically control the resource usage of LSS tasks under overload situations in an effort to maintain deterministic execution of HSS tasks; and b) for power/energy conservation. Some of recently proposed techniques for energy saving scheduling in multicore systems as in [13-17] will be investigated.

3. The comparative analysis will be done using the Freescale P4080 multi-core platform under a mix of HSS and LSS tasks from benchmark suites such as the MRTC WCET and EEMBC benchmarks.

NOVELTY:

While cache locking, partitioning and partition management mechanisms are not new concepts, there is no study/research applying to mixed-criticality workloads executing in virtualized environments on the Freescale P4080 platform.

POTENTIAL BENEFITS TO INDUSTRY MEMBERS:

The results of the proposed project will provide the basis for safe execution of mixed-criticality workloads on multi-core architectures with support for virtualization.

DELIVERABLES:

The deliverables for this project during the second year are as follows:

1. A comparative study of cache locking policies for given end-use scenarios on the Freescale P4080 platform.
2. A study of dynamic pausing/resuming of partitions (i.e., partition scheduling) to handle overload situations and for power/energy conservation.
3. Modified hypervisor and operating system source code, if any.

TIMELINE/MILESTONES: (PER QUARTER)

The timeline for the first four quarters of this project is as follows:

1. Quarter 1: Exploration of existing research in the area of cache locking and partitioning.
2. Quarter 2: Workload characterization and end-use scenario analysis under cache locking and partitioning schemes.
3. Quarter 3: (a) exploration of mechanisms to create and configure manager partitions;
   (b) comparative study of techniques for dynamic resource management using manager partitions.
4. Quarter 4: Report writing and technology transfer.

TECHNOLOGY TRANSFER:

Technology transfer will be performed in the form of comprehensive reports and updated hypervisor and operating system software.

BUDGET:

Funds in the amount of $25,000 are requested for:

1. Yearlong support of two graduate students
2. Travel to Industrial Advisory Board (IAB) meetings and member company locations for in-person meetings as required

BIBLIOGRAPHY: (ATTACH IN IEEE CONFERENCE OR JOURNAL FORMAT)

1. S. Xi, J. Wilson, C. Lu and C. Gill. “RT-XEN: Towards Real-Time Hypervisor Scheduling in Xen.” In Proceedings of the 9th ACM international conference on Embedded Software (EMSOFT), 2011.
2. R. Fuchsen. “How to address certification for multi-core based IMA platforms: Current status and potential solutions.” In Proceedings of the Digital Avionics Systems Conference (DASC), 2010.
3. C. Ault. “Challenges of safety-critical multi-core systems.” White paper, Wind River Research.
4. P. Baltham, et al. “Xen and the art of Virtualization,” In Proceedings of SOSP '03 19th ACM Symposium on Operating systems principles.
5. Jun Zhang; Kai Chen; Baojing Zuo; Ruhui Ma; Yaozu Dong; Haibing Guan. “Performance analysis towards a KVM-Based embedded real-time virtualization architecture.” 5th International Conference on Computer Sciences and Convergence Information Technology (ICCIT), 2010 , pp. 421 – 426.
6. M. Peshave. “High-Assurance Reconfigurable Multicore Processor Based Systems.” In Proceedings of the 13th IEEE International Symposium on High-Assurance Systems Engineering (HASE), 2011.
7. M.S. Mollison, J.P. Erickson, J.H. Anderson, S.K. Baruah and J.A. Scoredos. “Mixed-Criticality Real-Time Scheduling for Multicore Systems.” In Proceedings of the 10th IEEE International Conference on Computer and Information Technology (CIT), 2010.
8. Freescale Inc. “P4080: QorIQ P4080 Eight-Core Communications Processors with Data Path.” www.freescale.com/webapp/sps/site/prod_summary.jsp?code=P4080.
9. devicesolutions.net “Topaz i.MX25 CPU Module Technical Reference Manual.” http://devicesolutions.net/LinkClick.aspx?fileticket=hS62BQTuyhM%3D&tabid=305
10. Adventium Labs. “MiCART – Mixed-Criticality, Real-Time Virtualization Support.” www.adventiumlabs.com/?q=productsandservices/micart.

11. “Lmbench – Tools for Performance Analysis.” http://www.bitmover.com/lmbench/.
12. “MRTC WCET Benchmarks.” www.mrtc.mdh.se/projects/wcet/benchmarks.html.
13. I. Puaut and D. Decotigny. “Low-complexity algorithms for static cache locking in multitasking hard real-time systems.” In In IEEE Real-Time Systems Symposium, pages 114–123, 2002.
14. W. Y. Lee, “Energy-saving DVFS Scheduling of Multiple Periodic Real-time Tasks on Multicore Processors,” Proc. 13th IEEE/ACM Inter. Symp. Distributed Simulation and Real Time Applications, 2009, pp. 216–223..
15. S.-L. Chu, S.-R. Chen, S.-F. Weng, “Design a Low-Power Scheduling Mechanism for a Multicore Android System,” Fifth International Symposium on Parallel Architectures, Algorithms and Programming, 2012, pp. 25-30.
16. N. Iqbal, M.A. Siddique, J. Henkel, “SEAL: Soft error aware low power scheduling by Monte Carlo state space under the influence of stochastic spatial and temporal dependencies,” Proc. 48th ACM/EDAC/IEEE Design Automation Conference (DAC), 2011, pp. 134 – 139.
17. J. Lee,Y. B. Yun, K.G. Shin, “Reducing Peak Power Consumption in Multi-Core Systems without Violating Real-Time Constraints,” IEEE Transactions on Parallel and Distributed Systems, v. 25 , n. 4, pp. 1024 – 1033, 2014 .

I/UCRC Executive Summary - Project Synopsis		Date: 03/31/14
Project Title: Towards Predictable Execution of Safety-Critical Tasks on Mixed-Criticality Multi-Core Platforms.		
Center/Site: Center for Embedded Systems/Southern Illinois University Carbondale		
Principle Investigator: Dimitri Kagaris Harini Ramaprasad		**Type: Continuing**
Tracking No.: (CES office to input)	**Phone :** 618-453-7973 618-453-4755	**E-mail :** kagaris@engr.siu.edu harinir@siu.edu
		Proposed Budget: $20,000

Abstract: Multi-core architectures are a natural choice for integrating multiple independent functionalities into a single node in a cost- and space-effective manner. However, for systems with multiple levels of criticality, transporting highly safety-sensitive (HSS) applications (such as those for avionics systems with Design Assurance Level (DAL) of grade from DAL-C to DAL-A) onto a multi-core platform and sharing the benefits of the new computing environment with other less safety-sensitive (LSS) applications that have lower assurance levels but may be computation-intensive presents challenging problems in ensuring predictability/determinism of the HSS applications while still maintaining acceptable Quality of Service (QoS) for the LSS applications. The dominant approach towards isolating HSS and LSS tasks is the use of a virtualization environment (hypervisor) on top of the underlying multi-core platform. In prior work, extensive experimentation was conducted on the Freescale P4080 platform to characterize the behavior of HSS tasks in the presence of LSS tasks when executing them on different, statically derived partitions residing on separate cores. The goals of the proposed project are to apply the results of this characterization to end-use scenarios and to develop policies to exploit hardware mechanisms such as cache locking, cache partitioning and message passing among partitions to maintain determinism of HSS applications under regular and overload situations while maintaining QoS for the LSS applications.

Problem: Deterministic execution of HSS tasks in the presence of LSS tasks and other HSS tasks is challenging. The goal of this project is to develop policies to maintain responsiveness of HSS applications under regular and overload situations.

Rationale / Approach: The PIs propose to employ the following approach to achieve the goals of the proposed project: 1) Cache locking and partitioning are effective techniques to improve the predictability of HSS tasks and several policies for the same have been proposed. The PIs propose to explore the application of policies such as *minimize utilization* (Lock-MU) and *minimize interferences* (Lock-MI) [13] to end-use scenarios, identified by the workload characterization conducted in prior work. 2) Hypervisors typically allow configuration of one partition as a manager, giving this partition rights to pause and resume other partitions. The PIs propose to explore the use of such a manager partition a) to dynamically control the resource usage of LSS tasks under overload situations in an effort to maintain deterministic execution of HSS tasks and b) for power/energy conservation. Some of recently proposed techniques for energy saving scheduling in multicore systems as in [13-17] will be investigated and compared on the Freescale P4080 multi-core platform under a mix of HSS and LSS tasks from benchmark suites such as the MRTC WCET and EEMBC benchmarks.

Novelty: While cache locking, partitioning and partition management mechanisms are not new concepts, there is no study/research applying these in a safe manner to mixed-criticality workloads executing in virtualized environments on multi-core architectures.

Potential Member Company Benefits: The results of the proposed project will provide the basis for safe execution of mixed-criticality workloads on multi-core architectures with support for virtualization.

Deliverables for the proposed year: The deliverables for this project during the second year are as follows: 1) A comparative study of cache locking policies for given end-use scenarios on the Freescale P4080 platform. 2) A study of dynamic pausing/resuming of partitions (i.e., partition scheduling) to handle overload situations and for power/energy conservation. 3) Modified hypervisor and operating system source code, if any.

Milestones for the proposed year: Q1: Exploration of existing research in the area of cache locking and partitioning. Q2: Workload characterization and end-use scenario analysis under cache locking and partitioning schemes. Q3: a) exploration of mechanisms to create and configure manager partitions; b) development of strategies for dynamic resource management using manager partitions.

Progress to Date: THIS SECTION TO BE UPDATED IN JANUARY

Estimated Start Date: 08/15/2014	**Estimated Knowledge Transfer Date**: 08/31/2015

PI INFORMATION: (ATTACH 2-PAGE CV)

Harini Ramaprasad

Department of Electrical and Computer Engineering Phone: (618) 453-4755
Southern Illinois University Carbondale Fax: (618) 453-7972
Carbondale, IL 62901-6603 E-mail: harinir@siu.edu

Professional Preparation

B.S. Computer Science, Bangalore University, Bangalore, India, 2001
M.S. Computer Science, North Carolina State University, Raleigh, North Carolina, 2006
Ph.D. Computer Science, North Caroline State University, Raleigh, North Carolina, 2008

Research Interests

Real-time/Embedded Systems, Cyber-Physical Systems Operating Systems, Computer Architecture, Compilers

Appointments

Aug 2008 - present Assistant Professor, Dept. of Electrical and Computer Engineering,
Southern Illinois University Carbondale, Carbondale, Illinois
2002 - 2008 Research Assistant, North Carolina State University, Raleigh, North Carolina

Honors and Awards

Outstanding Teacher in the Department of Electrical and Computer Engineering for the year 2011.

Related and Significant Products

1. S. Motakpalli, V.P. Jain, H. Ramaprasad. "Aperiodic Job Handling in Cache-Based Real-Time Systems." In Proc. of the International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA), 2013.
2. A. Choudhari, H. Ramaprasad, T. Paul, J. Kimball, M. Zawodniok, B. McMillin and S. Chellappan. "StabilityA. Choudhari, H. Ramaprasad, T. Paul, J. Kimball, M. Zawodniok, B. McMillin and S. Chellappan. "Stability of a Cyber-Physical Smart Grid Systems using Cooperating Invariants." To appear as a *full paper* in Proc. of the International Computer Software and Applications Conference (**COMPSAC**), 2013.
3. A. Sarkar, F. Mueller, H. Ramaprasad. "Static Task Partitioning for Locked Caches in Multi-Core Real-Time Systems." To appear in Proc. of the Conference on Compilers, Architecture and Synthesis for Embedded Systems (**CASES**), 2012.
4. O. Acevedo, D. Kagaris, K. Poluri, H. Ramaprasad and S. Warner. "Towards Optimal Design of Avionics Networking Infrastructures." In Proc. of the 31st Digital Avionics Systems Conference (**DASC**), 2012.
5. M. Shekhar, A. Sarkar, H. Ramaprasad and F. Mueller. "Semi-Partitioned Hard-Real-Time Scheduling Under Locked Cache Migration in Multicore Systems." In Proc. of the Euromicro Conference on Real-Time Systems (**ECRTS**), 2012.
6. A. Sarkar, F. Mueller and H. Ramaprasad. "Predictable Task Migration for Locked Caches in Multi-Core Systems". In Proc.of the ACM SIGPLAN Conference on Languages, Compilers and Tools for Embedded Systems (**LCTES**), 2011.
7. H. Ramaprasad and F. Mueller. "Tightening the Bounds on Feasible Preemptions". In Transactions on Embedded Computing Systems (**TECS**), Volume 10, Number 2, Article 27, December 2010.
8. A. Sarkar, F. Mueller, H. Ramaprasad and S. Mohan. "Push-Assisted Migration of Real-Time Tasks in Multi-Core Processors". In Proc. of the ACM SIGPLAN Conference of Languages, Compilers and Tools for Embedded Systems (**LCTES**), June 2009.

Synergistic Activities

Grant Review Panel Member

• National Science Foundation (NSF) – 2009, 2010, 2011, 2012

Program Chair

• Workshop on Energy-Aware Design and Analysis of Cyber-Physical Systems (**WEA-CPS**) – 2010

Track co-chair

• International Symposium on Electronic System Design (**ISED**) – 2011

Technical Program Committee member

• International Conference on Embedded Software (**EMSOFT**) – 2011

• Euromicro Conference on Real-Time Systems (**ECRTS**) – 2010, 2011, 2012, 2013

• Real-Time Systems Symposium (**RTSS**) – 2009, 2010, 2011, 2013

• International Conference on Embedded Computing (**EmbeddedCom**) – 2009

• Workshop on Cyber-Physical Systems (**WCPS**) – 2009

• International Conference on Embedded Software and Systems (**ICESS**) – 2009

• Real-Time and Embedded Technology and Applications Symposium (**RTAS**) – 2009, 2011

• International Symposium on Object and component-oriented Real-time distributed Computing (**ISORC**) – 2012, 2013

• International Conference on Embedded and Real-Time Computing Systems and Applications (**RTCSA**) – 2013

• International Conference on Real-Time Networks and Systems (**RTNS**) – 2013

External reviewer

• Real-Time and Embedded Technology and Applications Symposium (**RTAS**) – 2010

• Euromicro Conference on Real-Time Systems (**ECRTS**) – 2003, 2004, 2006, 2008, 2009

• IEEE Real-Time Systems Symposium (**RTSS**) – 2006, 2008

• Workshop on Worst-Case Execution Time Analysis (**WCET**) – 2006

• ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems (**LCTES**) – 2006, 2007, 2008

• IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (**RTCSA**) – 2006

• International Conference on Parallel and Distributed Systems (**ICPADS**) - 2006

• International Parallel and Distributed Processing Symposium (**IPDPS**) – 2009

• International Conference on Compilers, Architecture and Synthesis for Embedded Systems (**CASES**) – 2008, 2009

• ACM Transactions on Embedded Computing Systems (**TECS**)

• IEEE Transactions on Computers (**TC**)

• IEEE Transactions on Parallel and Distributed Systems (**TPDS**)

• ACM Transactions on Architecture and Code Optimization (**TACO**)

• Design Automation for Embedded Systems (**DAEM**)

Research Collaborators

• Frank Mueller (North Carolina State University)

• Yuan Xie (Penn State University)

• Aviral Shrivastava (Arizona State University)

• Jonathan Kimball, Maciej Jan Zawodniok, Bruce McMillin, Sriram Chellappan (Missouri University of Science and Technology**)**

• Spyros Tragoudas, Dimitrios Kagaris, Ning Weng, Haibo Wang (Southern Illinois University Carbondale)

• Wei Zhang (Virginia Commonwealth University)

Graduate Advisor

• Frank Mueller (North Carolina State University)

Thesis Advisor

• MS, Southern Illinois University Carbondale:

(Completed) Kedar Katre, Vardhman Jain Pukhraj Jain, Aravind Mysore Chandrashekar, Robin Rajkumar
(Current) Kaushik Poluri

• PhD, Southern Illinois University Carbondale:

(Current) Mayank Shekhar, Sankalpanand Motakpalli, SatyaMohan Raju Gudidevuni, Ashish Choudhari, Aishwarya Vasu, Kiriti Nagesh Gowda

PI INFORMATION: (ATTACH 2-PAGE CV)

Short Curriculum Vitae

DIMITRI KAGARIS
Professor
Department of Electrical & Computer Engineering
Southern Illinois University
Carbondale, IL 62901, USA
tel: (618)453-7973
fax: (618)453-7972
e-m: kagaris@engr.siu.edu

Dimitri Kagaris received the Diploma degree in Computer Engineering and Informatics from the University of Patras, Greece, in 1988, and the M.S. and Ph.D. degrees in Computer Science from Dartmouth College, Hanover, New Hampshire, USA, in 1991 and 1994, respectively.
He is currently a full professor in the Electrical & Computer Engineering Department, Southern Illinois University, Carbondale, Illinois, USA. His research interests include multicore systems, digital design automation and test, VLSI synthesis, computer networks.
He has over 80 publications in peer-reviewed journals and conferences and has contributed chapters in scientific encyclopedias. He has been active in the area of Built-in Self-Test and Design for Testability since 1992. Part of his research has been supported by National Science Foundation (NSF). He has received twice the Outstanding Paper Award from the IEEE International Conference on Computer Design. He has served as a reviewer in major journals and conferences and has participated three times in NSF panels for the review and funding of Design Automation proposals. He is currently serving as Associate Editor of the IEEE Transactions on Computers.

RECENT RELEVANT JOURNAL PUBLICATIONS

1. D. Kagaris, ``Maximizing the Lifetime of a Wireless Sensor Network with Fixed Targets,'' **Ad Hoc and Sensor Wireless Networks**, v. 17, n. 3-4, pp. 253 - 268, 2013.

2. D. Nikolos, D. Kagaris, S. Sudireddy, S. Gidaros, ``An Improved Search Method for Accumulator-Based Test Set Embedding,'' **IEEE Transactions on Computers**, v. 58, n. 1, pp. 132 - 138, Jan. 2009.

3. J. Kakade, D. Kagaris, D.K. Pradhan, ``Evaluation of Generalized LFSRs as Test Pattern Generators in Two-Dimensional Scan Designs,'' **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, v. 27, n. 9, pp. 1689 - 1692, Sept. 2008.

4. J. Kakade, D. Kagaris, “Minimization of Linear Dependencies through the Use of Phase

Shifters," **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,** v. 26, n. 10, pp. 1877-1882, Oct. 2007.

5. D. Kagaris, T. Haniotakis, ``A Methodology for Transistor-Efficient Supergate Design,'' **IEEE Transactions on VLSI Systems**,v. 15, n. 4, pp. 488-492, Apr. 2007.

6. D. Kagaris, ``Improved TDM Switching Assignments for Variable and Fixed Burst Length,'' **International Journal of Satellite Communications and Networking**, v. 25, pp. 93-107, 2007.

7. D. Kagaris, P. Karpodinis, D. Nikolos, ``A Method for Accumulator-Based Test-per-Scan BIST,'' **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, v. 25, n. 11, pp. 2578-2586, Nov. 2006.

8. D. Kagaris, S. Tragoudas, S. Kuriakose, "InTeRail: A Test Architecture for Core-Based SOCs," **IEEE Transactions on Computers**, v. 55, n. 2, pp. 137-149, Feb. 2006.

9. D. Kagaris, "Phase Shifter Merging," **Journal of Electronic Testing: Theory and Applications**, vol. 21, n. 2, pp. 161-168, April 2005.

10. D. Kagaris, "A Unified Method for Phase Shifter Computation**," ACM Transactions on Design Automation of Electronic Systems**, vol. 10, no. 1, pp. 157-167, Jan. 2005.

11. D. Kagaris, "Multiple-Seed TPG Structures," **IEEE Transactions on Computers**, vol. 52, no. 12, pp. 1633-1639, Dec. 2003.

12. D. Kagaris, S. Tragoudas "On the Non-Enumerative Path Delay Fault Simulation Problem," **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, vol. 21, n. 9, pp. 1095-1100, Sep. 2002.

13. D. Kagaris, "Linear Dependencies in Extended LFSMs," **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, vol. 21, n. 7, pp. 852-858, July 2002.