| I/UCRC Executive Summary - Project Synopsis | | Date: 03/31/2014 |
|---|---|---|
| **Project Title:** A Layout-Aware Methodology for Path-Delay Fault Grading and Diagnosis | | |
| **Center/Site**: NSF I/UCRC for Embedded Systems, SIUC site | | |
| **Principle Investigators: Spyros Tragoudas, Themistoklis Haniotakis** | | **Type: New** |
| **Tracking No**.: | **Phone :** (618 )453 - 7027 | **E-mail : spyros@engr.siu.edu, haniotak@engr.siu.edu** |
| | | **Proposed Budget**: $50,000 |

**Abstract**:
The deep-submicron effects are becoming more prominent with technology scaling and thereby, pose new challenges for effective grading and diagnosis of faults. Guaranteeing coverage for various abnormalities in an Integrated Circuit(IC) is a daunting task. Proposed here is a methodology to perform a layout-aware grading for Path Delay Faults (PDF) so as to characterize path criticalities based on each path's sensitivity to a given set of parameters. Furthermore, to diagnose potential failures that can result due to variations in a parameter or a set of parameters.

**Problem**:

1. Implicit layout-aware grading of path-delay faults.
2. Characterizing path criticalities based on layout information.
3. Diagnosis of potential faults with respect to a target parameter.

**Rationale / Approach**:

1. With continued scaling of devices and interconnects the behavior of an Integrated Circuit (IC) has become more sensitive to manufacturing processes, environmental variations and other uncertainties.
2. Certain uncertainties such as power supply noise and crosstalk, which are pattern dependent, contribute to the worsening signal integrity issues in modern ICs.
3. The quality of a test set should be determined not only by the timing behavior of the paths detected by the test set but also the sensitivity of such paths to the variations in process and environmental parameters.
4. Failure analysis/Diagnosis should be able to leverage layout information in order to identify potential defects.
5. We propose to determine the quality of a given test set in identifying the defects arising from process and environmental variations.
6. Additionally, we propose to build an infrastructure that can perform effective diagnosis using information from the layout.

**Novelty**:

1. Non enumerative grading for PDFs and implicitly annotating paths with layout information.
2. Metrics to determine test set quality using layout information.
3. Effective failure analysis using layout information.

**Potential Member Company Benefits:**

1. A layout-aware path grading tool to estimate the quality of a given test set.
2. A new layout-aware metric for calculating test set quality.
3. A tool for effective failure analysis by leveraging layout information.

**Deliverables for the proposed year:**

1. Software tool to perform layout-aware path grading and thereby, estimate test set quality.
2. Software tool to aid failure analysis using layout information.

| **Estimated Start Date**: 08/16/2014 | **Estimated Knowledge Transfer Date**: 08/16/2015 |
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**Center for Embedded Systems (CES)**
**Request for Proposals Template – YEAR 6**

**DUE: Monday, March 31, 2014, by 5 p.m.**

| | | | | | |
|---|---|---|---|---|---|
| **TITLE:** | A Layout-Aware Methodology for Path-Delay Fault Grading and Diagnosis | | | | |
| **PIs:** | Spyros Tragoudas<br>Themistoklis Haniotakis | **EMAIL:** | spyros@engr.siu.edu<br>haniotak@engr.siu.edu | **TEL:** | 618-453-7027 |
| **DEPT:** | ECE | **SCHOOL:** | SIUC | | |


**ABSTRACT: (250 OR FEWER WORDS)**

The deep-submicron effects are becoming more prominent with technology scaling and thereby, pose new challenges for effective grading and diagnosis of faults. Guaranteeing coverage for various abnormalities in an Integrated Circuit(IC) is a daunting task. Proposed here is a methodology to perform a layout-aware grading for Path Delay Faults (PDF) so as to characterize path criticalities based on each path's sensitivity to a given set of parameters. Furthermore, to diagnose potential failures that can result due to variations in a parameter or a set of parameters.


**PROBLEM:**

1. Implicit layout-aware grading of path-delay faults.
2. Characterizing path criticalities based on layout information.
3. Diagnosis of potential faults with respect to a target parameter.

**RATIONALE:**

1. With continued scaling of devices and interconnects the behavior of an Integrated Circuit (IC) has become more sensitive to manufacturing processes, environmental variations and other uncertainties.
2. Certain uncertainties such as power supply noise and crosstalk, which are pattern dependent, contribute to the worsening signal integrity issues in modern ICs
3. Failure to consider signal integrity issues during test pattern generation could lead to in-field reliability issues and yield loss due to functional or timing related failures [5]
4. Considering for such variations during the Automatic Test Pattern Generation (ATPG) is extremely difficult.
5. The quality of a test set should be determined not only by the timing behavior of the paths detected by the test set but also the sensitivity of such paths to the variations in process and environmental parameters.
6. Failure analysis/Diagnosis should be able to leverage layout information in order to identify potential defects.

**APPROACH:**

In the previous year we proposed and implemented an infrastructure for PDF grading using transition and functional test patterns. Also proposed, was a methodology to identify critical uncovered defects and generate tests to target such defects using the PDF model. Continuing on this effort, this year we propose a methodology for grading of PDFs using layout information. Essentially, we propose to determine the quality of a given test set in identifying the defects arising from process and environmental variations. Additionally, we propose to build an infrastructure that can perform effective diagnosis using information from the layout.
Consider two paths Path-A and Path-B which are equally critical in terms of their timing behavior. However, only one of the two paths, Path-A, exhibits a higher sensitivity to a process parameter *p*. If this process parameter *p* were

susceptible to a higher degree of variation in the given IC then the criticality of Path-A must be ranked higher than that of Path-B. A test set must include patterns to test Path-A by exciting the maximum delay along Path-A.
Recent work in [4] presents a test pattern generation method that would generate a pattern to excite the longest delay along a path by introducing crosstalk and power supply noise effects. The work in [5] characterizes the different patterns available for a path based on their ability to produce crosstalk and power supply noise effects. They do so by avoiding simulation and develop a layout based metric to grade the quality of the pattern. The intensions of the authors in [4] and [5] was to generate test patterns considering signal integrity effects only and therefore, provide little assistance towards diagnosing potential faults using layout information.
In our previous work [1], we showed how each path in a ZBDD can be annotated with statistical delays by operating in a path-implicit manner. Our work in [2] [3] introduced methodologies for implicit and exact PDF grading using the ZBDD data structure. In the proposed work, we leverage [1] and [2] to implicitly build a database of paths detected by a given test set and annotate paths with information to reflect each path's sensitivity to different layout parameters. Such an infrastructure could prove to be of great help during failure analysis. Essentially, if one was interested in identifying all such paths that could potentially exhibit defect behavior due to variations of a parameter *p* then one can quickly grab such paths from the database by performing a few implicit operations to select paths with a high degree of sensitivity to *p*.

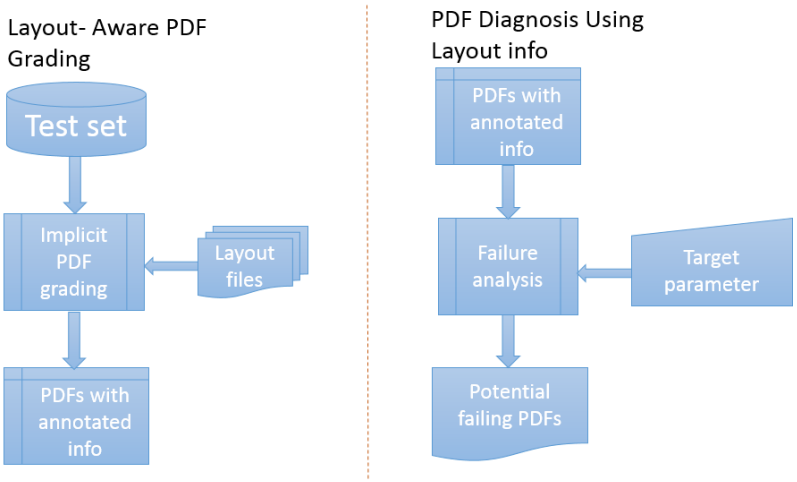


Figure 1: Proposed flow for layout-aware grading and diagnosis

**NOVELTY:**

1. Non enumerative grading for PDFs and implicitly annotating paths with layout information.
2. Metrics to determine test set quality using layout information.
3. Effective failure analysis using layout information.

**POTENTIAL BENEFITS TO INDUSTRY MEMBERS:**

1. A layout-aware path grading tool to estimate the quality of a given test set.
2. A new layout-aware metric for calculating test set quality.
3. A tool for effective failure analysis by leveraging layout information.

**DELIVERABLES:**

1. Software tool to perform layout-aware path grading and thereby, estimate test set quality.
2. Software tool to aid failure analysis using layout information.

**TIMELINE/MILESTONES: (PER QUARTER)**

**First half:**

- Software tool to perform layout-aware path grading and thereby, estimate test set quality.

**Second half:**

- Software tool to aid failure analysis using layout information.

**TECHNOLOGY TRANSFER:**

- Software tools developed during the course of this project will be transferred to the member company.
- Submission to peer-reviewed conference and journals.

**BUDGET:**

**Cost of $50,000**

- Support a graduate student for up to 25%.
- Partial support for the PIs.
- Travel to member company and conferences to present research findings.

**BIBLIOGRAPHY: (ATTACH IN IEEE CONFERENCE OR JOURNAL FORMAT)**


[1] Somashekar A.M, Tragoudas S, Gangadhar S, Jayabharathi R, "Non-enumerative generation of statistical path delays for ATPG," In *Proceedings of the 30th IEEE International Conference on Computer Design (ICCD),* pp.514, 515, Sept. 30 2012-Oct. 3 2012.

[2] Kumar M.M.V., Tragoudas S, Chakravarty S, Jayabharathi R, "Exact Delay Fault Coverage in Sequential Logic Under Any Delay Fault Model," In *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol.25, no.12, pp.2954-2964, Dec. 2006.

[3] Kumar M.M.V., Tragoudas S, Chakravarty S, Jayabharathi R, "Implicit and exact path delay fault grading in sequential circuits," In *Proceedings of the Design, Automation and Test in Europe*, pp.990,995, March 2005.

[4] Ma J, Lee J, Tehranipoor M, "Layout-aware pattern generation for maximizing supply noise effects on critical paths", In *Proceedings of IEEE VLSI test symposium* (VTS'09), pp. 221,226.

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# SPYROS TRAGOUDAS

## PROFESSIONAL AFFILIATION AND CONTACT INFORMATION

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## EDUCATION

*1986* Diploma (5 years), Computer Engineering and Informatics Department, University of Patras, Greece

*1988* M.S., Erik Jonsson School of Engineering and Computer Science, Computer Science Program, The University of Texas at Dallas, Richardson, TX 75083-0688.

*1991* Ph.D., Erik Johnson School of Engineering and Computer Science, Computer Science Program, The University of Texas at Dallas, Richardson, TX 75083-0688.

## PROFESSIONAL EXPERIENCE

*07/01/12 – current* Professor and Chair, Electrical & Computer Eng. Dept., Southern Illinois University Carbondale

*03/01/09-current* Director, NSF IUCRC on Embedded Systems, SIUC-site.

*07/16/99- current* Professor, Electrical & Computer Eng. Dept., Southern Illinois University Carbondale.

*08/16/98-07/15/99* Associate Professor, Electrical and Computer Engineering Department, University of Arizona.

*08/16/91-08/15/98* Associate Professor, Computer Science Department, Southern Illinois University Carbondale (Assistant Professor until 6/30/96).

*07/01/97-08/15/98* Graduate Program Director, Computer Science Department, Southern Illinois University Carbondale.

*01/03/87-08/14/91* Research/Teaching Assistant, Computer Science Program, School of Engineering and Computer Science, The University of Texas at Dallas, Richardson, TX 75083-0688.

*08/15/86-01/02/87* Systems Analyst, Computer Technology Institute, Patras, Greece.

## RESEARCH INTERESTS

Design and Test Automation for VLSI, Embedded Systems

## RESEARCH SPONSORS

*Direct support:* National Science Foundation, US Navy, SAIC, Intel, Qualcomm, Synopsys

*NSF IUCRC:* NSF, NAVSEA Crane, Rockwell Collins, United Technologies Aerospace Systems, SAIC, Intel, Caterpillar, TSI, EMAC, Wildlife Materials

## PROFESSIONAL SERVICE

*Editorial Board:* IEEE Transactions on Computers, VLSI Design journal, Journal of electrical and Computer Engineering, Universal Computer Science, Research Letters in Electronics.

General Chair of IEEE DFTS 2010, Program Committee Chair of DFTS 2009, Program Committee member of many International Conferences

Has graduated 14 PhD students and supervised over 60 MS theses. Currently advising 11 PhD students

**PUBLICATIONS**

Over 70 journal papers and over 130 articles in peer-reviewed conference proceedings

*Ten recent journal publications*

• A.K. Palaniswamy and S.Tragoudas, An Efficient Heuristic to Identify Threshold Logic Functions, ACM Journal on Emerging Technologies in Computing (JETC), to appear in 2012.

• M.N. Skoufis, S. Tragoudas, An on-line Failure Detection Method for Data Buses using Multi-threshold Receiving Logic, IEEE Transactions on Computers, vol. 61, no. 2, pp. 187-198, Feb. 2012

• K. Stewart, Th. Haniotakis, and S. Tragoudas, Securing sensor networks: A novel approach that combines encoding, uncorrelation, and node disjoint transmission, Ad Hoc Networks, vol. 10, issue 3, May 2012, pp. 328-328, Elsevier.

• M.N. Skoufis, K. Karmakar, S. Tragoudas, and T. Haniotakis, A data capturing method for buses on chip, IEEE Transactions on Circuits and Systems I, vol. 57, no. 7, pp.1631-1641, July 2010.

• D. Jayaraman, R. Sethuram, and S. Tragoudas, Scan Shift Power Reduction by Gating Internal Nodes. J. Low Power Electronics 6(2): 311-319 (2010).

• E. Flanigan, S, Tragoudas, Path Delay Measurement Techniques using Linear Dependency Relationships, IEEE Transactions on VLSI Systems, vol. 18, issue 6, pp.1011-1015, June 2010.

• R. Adapa, S. Tragoudas, Techniques to Prioritize Paths for Diagnosis, IEEE Transactions on VLSI Systems, vol. 18, issue 4, pp. 658-661, April 2010.

• K. Christou, M. K. Michael, and S. Tragoudas, On the Use of ZBDDs for Implicit and Compact Critical Path Delay Fault Test Generation, Journal of Electronic Testing: Theory and Applications, 2008.

• A. Abdulrahman and S. Tragoudas, Low-Power Multi-Core ATPG to Target Concurrency, Integration, the VLSI Design Journal, vol. 41, issue 4, pp. 459-473, July 2008.

• C. Song, S. Tragoudas, Identification of Critical Executable Paths at the Architectural Level, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), vol. 27, no. 12, pp. 2291-2302, December 2008

# THEMISTOKLIS HANIOTAKIS

## PROFESSIONAL AFFILIATION AND CONTACT INFORMATION

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## EDUCATION

| | | |
|---|---|---|
| Ph.D. | [1998] | Department of Informatics, University of Athens, Greece |
| Bachelor | [1991] | Department of Physics, University of Athens, Greece |

## PROFESSIONAL EXPERIENCE

| | |
|---|---|
| [Fall Semester 2013] | Associate Professor, Department of Electrical and Computer Engineering, Southern Illinois University at Carbondale. |
| [2011- Spring 2013] | Tenured Assistant Professor Department of Computer Engineering and Informatics, University of Patras, Greece |
| [Fall Semester 2011] | Sabbatical leave as a Visiting Assistant Professor, Department of Electrical and Computer Engineering, Southern Illinois University at Carbondale. |
| [2007-2011] | Assistant Professor Department of Computer Engineering and Informatics, University of Patras, Greece |
| [2001-2007] | Assistant Professor Department of Electrical and Computer Engineering, Southern Illinois University at Carbondale. |
| [2000-2001] | Visiting Assistant Professor Department of Electrical and Computer Engineering, Southern Illinois University at Carbondale. |
| [1999-2000] | Visiting Assistant Professor Department of Computer Engineering and Informatics, University of Patras, |
| [1998-1999] | Engineer, Low Power & Low Voltage group, ISD Corp. Greece. |
| [1996-1997] | Served in the Greek army. |
| [1991-1995] | Research Center "Demokritos", Institute of Informatics & Telecommunications, Greece. |

## RESEARCH INTERESTS

VLSI Design & Test, Low-Power & RF VLSI Design

## RESEARCH SPONSORS

European Union/Greek government, Intel, Qualcomm.

## PROFESSIONAL SERVICE

Program Committee member for International On-Line Testing Workshop [2000-2002] International On-Line Testing Symposium [2003-2007], Asia Symposium on Quality Electronic Design ASQED [2010-2013].
Reviewer for numerous Conferences and Journals.
Has supervised 12 MS Thesis.

## PUBLICATIONS

20 journal paper and over 45 articles in peer-reviewed proceedings

Ten Recent journal publications


[1] "Domino CMOS SCD/SFS 2-out-of-3 and 1-out-of-3 Code Checkers" Th. Haniotakis, Y. Tsiatouhas, C. Efstathiou and D. Nikolos, "Domino-CMOS Strongly Code Disjpoint and Strongly Fault Secure 2-out-of-3 and 1-out-of-3 Code Checkers", International Journal of Electronics, vol. 90, no. 2, pp. 145-158, 2003.

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[3] "A Circuit for Concurrent Detection of soft and Timing Errors in Digital CMOS ICs" S. Matakias, Y. Tsiatouhas, A. Arapoyanni and Th. Haniotakis, Journal of Electronic Testing: Theory and Applications 20, pp. 523-531, 2004.

[4] "A Design Technique for Energy Reduction in NORA CMOS Logic" K. Limniotis, Y. Tsiatouhas, T. Haniotakis A. Arapoyanni, IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications. Volume 53, Issue 12, Dec. 2006 pp. 2647-2655

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[8] "A Current Mode, Parallel, Two-Rail Code Checker" S. Matakias, Y. Tsiatouhas, T. Haniotakis, A. Arapoyanni, IEEE Transactions on Computers. Volume 57, Issue 8, Aug. 2008 pp. 1032-1045

[9] "A Data Capturing Method for Buses on Chip" M. Skoufis, K. Karmakar, S. Tragoudas, T. Haniotakis IEEE Transactions on Circuits and Systems I: Regular Papers. Volume 57, Issue 7, 2010 pp. 1631-1641.

[10] "Securing sensor networks: A novel approach that combines encoding, uncorrelation and node disjoint transmission", Khadija Stewart, Themistoklis Haniotakis, Spyros Tragoudas, Ad Hoc Networks, Volume 10, Issue 3, May 2012, Pages 328–338