Center for Embedded Systems (CES)
Request for Proposals Template – YEAR 6

TITLE:	Comparison of Image Processing Algorithms on Micro-Array Architectures and GPGPU Platforms				
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ABSTRACT: (250 OR FEWER WORDS)

The proposed project is a study analyzing the performance of image processing algorithms on General-Propose computing on Graphics Processing Units (GPGPU) architecture in comparison to a micro-core array embedded processor. The project will create a set of metrics which will measure speed, power consumption, and cost. The metrics will provide an exact analysis of the trade-offs between the different architectures. Furthermore, the study will determine feasibility for processing real-time video information of high resolution video streams.

Additionally, an investigation into the performance of several image processing algorithms such as a noise reduce, will be performed. A core objective will be to select several image processing algorithms and optimize them for the GPGPU environment. Analysis of the performance gains and trade-offs will be included in the final survey.

PROBLEM:

Many studies have shown a reduction in execution time when implementing image processing algorithms on GPGPUs [1] [2]. However, there is no comprehensive survey which examines the trade-off between power, performance and cost for implementation compared to an embedded system due to the power required by GPGPU systems. However, newer mobile versions of the GPGPU platforms begun to appear on the market changing the traditional role of GPGPU computing, and no quantification has been made comparing these to current embedded processors.

RATIONALE:

While traditional discrete graphic cards consume a lot of power compared to the general CPU, the landscape of the GPGPU platform is changing [1]. The integrated GPGPU capability is now appearing in low power mobile devices. These devices have fewer cores running at slower clock speeds than the desktop discrete GPU units, but also consume considerably less power. This leads to a greater number of design choices for an embedded system's developer.

The use of image sensors in embedded systems has increased dramatically in recent years. Cameras, cars, drones, planes and many other platforms have deployed these sensors for data collection and safety critical systems. There are two criteria that are common for these applications. The system has real-time constraints that must be met, and the system must consume a low amount of power. Therefore there is high demand by developers to know which platforms meet their system requirements.

APPROACH:

There are two major GPGPU platforms that can be targeted for migration of the tool, CUDA [3] and OpenCL [4]. It has been show there are trade-offs between using CUDA which generally has higher performance, and OpenCL which has greater hardware support and considered more portable [5]. NVIDIA is also currently moving the GPGPU technology into the mobile market with their Tegra platform. A survey of the various GPGPU platforms will be conducted which will look at the availability, portability, cost, power and performance characteristics of each [6] [7].

After the survey is complete, two GPGPU platforms will be selected for benchmarking, one being a desktop based GPGPU, the other being a mobile based GPGPU. The GPGPU platforms will be compared with an in-house Micro-core array architecture used in current embedded systems. With emphasis on image processing algorithms such as noise reduction, several algorithms will be selected for implementation on the platforms. An effort will be made to optimize the algorithms for the various platforms to maximize the parallelism. Using the selected the characteristics of the image processing algorithms will be recorded using a well-defined set of metrics. Documentation and conclusions of the survey will be compiled into a final report made available to the consortium.

NOVELTY:

Current work has been focused on the performance gains using GPGPU technology in desktop graphics processing units. This work will examine the performance/power trade-offs as well as investigate upcoming low power mobile GPGPU platforms such as NIVIDIA's Tegra K1. Furthermore, the work will lead to more optimized image processing algorithms for GPGPU systems.

POTENTIAL BENEFITS TO INDUSTRY MEMBERS:

GPGPU platforms have primarily been deployed for computing large datasets using highly parallel algorithms. With the more powerful GPGPU hardware requiring upwards of 200 watts of power, this hardware has not typically been thought of as a solution for power conservative embedded systems. However, mobile devices have created a demand for low power integrated graphics with GPGPU capabilities to offload some of the computation from the main processor.

As such, a reassessment of GPGPU platforms could lead to future incorporation of GPGPU technologies in embedded system platforms. This will result in more powerful and accurate analysis of real-time sensor data. With further investigation into the image processing domain could yield more power efficient vision algorithms which would have an impact on robotic manufacturing and transportation systems which are rapidly incorporating vision sensors.

DELIVERABLES:

- Survey of GPGPU Platforms
- Comparison Study of the embedded system and GPGPU Platforms
- Optimized Image Processing Algorithms

TIMELINE/MILESTONES: (PER QUARTER)

- Select GPGPU Platforms (8/31/2014)
- Select a set of image processing algorithms (9/30/2014)
- Implement and optimize image processing algorithms on GPGPU platform (12/20/2014)
- Port algorithms to a multi-core embedded system (3/31/2015)
- Perform an Analysis on the performance difference between the platforms (7/31/2015)

TECHNOLOGY TRANSFER:

Biweekly teleconferences with the industrial liaisons will occur throughout the duration of the project to ensure deliverables are met and within scope.

BUDGET:

$25,000 is requested to support the PIs and two graduate students, and to purchase demonstration hardware and software tools.

BIBLIOGRAPHY: (ATTACH IN IEEE CONFERENCE OR JOURNAL FORMAT)

[1] E. Fykse, "Performance Comparison of GPU, DSP and FPGA implementations of image processing and computer vision algorithms in embedded systems," Norwegian University of Science and Technology, 2013.

[2] S. Rogmans, M. Dumont, G. Lafruit and P. Bekaert, "Migrating real-time depth image-based rendering from traditional to next-gen GPGPU," in *3DTV Conference: The True Vision - Capture , Transmission and Display of 3D Video*, 2009.

[3] "CUDA Toolkit Documents," 2014. [Online]. Available: http://docs.nvidia.com/cuda/.

[4] "The open standard for parallel programming of heterogeneous systems, OpenCL 2.0," 2014. [Online]. Available: https://www.khronos.org/opencl/.

[5] Jianbin Fang, A. Varbanescu and H. Sips, "A Comprehensive Performance Comparison of CUDA and OpenCL," in *International Conference on Parallel Processing (ICPP)*, 2011.

[6] N. Goswami, R. Shankar, M. Joshi and Tao Li, "Exploring GPGPU Workloads: Characterization methodology, analysis and microarchitecture," in *IEEE International Symposium on Workload Characterization*, 2010.

[7] Jianming Pan and Yangdong Deng, "Charaterizing the Execution Dynamics of GPGPU Applications," in *Fifth International Conference on Computational and Information Sciences (ICCIS)*, 2013.

PI INFORMATION: (ATTACH 2-PAGE CV)

SPYROS TRAGOUDAS

PROFESSIONAL AFFILIATION AND CONTACT INFORMATION

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EDUCATION

1986 Diploma (5 years), Computer Engineering and Informatics Department, University of Patras, Greece

1988 M.S., Erik Jonsson School of Engineering and Computer Science, Computer Science Program, The University of Texas at Dallas, Richardson, TX 75083-0688.

1991 Ph.D., Erik Johnson School of Engineering and Computer Science, Computer Science Program, The University of Texas at Dallas, Richardson, TX 75083-0688.

PROFESSIONAL EXPERIENCE

07/01/12 – current Professor and Chair, Electrical & Computer Eng. Dept., Southern Illinois University Carbondale

03/01/09-current Director, NSF IUCRC on Embedded Systems, SIUC-site.

07/16/99- current Professor, Electrical & Computer Eng. Dept., Southern Illinois University Carbondale.

08/16/98-07/15/99 Associate Professor, Electrical and Computer Engineering Department, University of Arizona.

08/16/91-08/15/98 Associate Professor, Computer Science Department, Southern Illinois University Carbondale (Assistant Professor until 6/30/96).

07/01/97-08/15/98 Graduate Program Director, Computer Science Department, Southern Illinois University Carbondale.

01/03/87-08/14/91 Research/Teaching Assistant, Computer Science Program, School of Engineering and Computer Science, The University of Texas at Dallas, Richardson, TX 75083-0688.

08/15/86-01/02/87 Systems Analyst, Computer Technology Institute, Patras, Greece.

RESEARCH INTERESTS

Design and Test Automation for VLSI, Embedded Systems

RESEARCH SPONSORS

Direct support: National Science Foundation, US Navy, SAIC, Intel, Qualcomm, Synopsys

NSF IUCRC: NSF, NAVSEA Crane, Rockwell Collins, United Technologies Aerospace Systems, SAIC, Intel, Caterpillar, TSI, EMAC, Wildlife Materials

PROFESSIONAL SERVICE

Editorial Board: IEEE Transactions on Computers, VLSI Design journal, Journal of electrical and Computer Engineering, Universal Computer Science, Research Letters in Electronics.

General Chair of IEEE DFTS 2010, Program Committee Chair of DFTS 2009, Program Committee member of many International Conferences

Has graduated 14 PhD students and supervised over 60 MS theses. Currently advising 11 PhD students

PUBLICATIONS

Over 70 journal papers and over 130 articles in peer-reviewed conference proceedings

Ten recent journal publications

• A.K. Palaniswamy and S.Tragoudas, An Efficient Heuristic to Identify Threshold Logic Functions, ACM Journal on Emerging Technologies in Computing (JETC), to appear in 2012.

• M.N. Skoufis, S. Tragoudas, An on-line Failure Detection Method for Data Buses using Multi-threshold Receiving Logic, IEEE Transactions on Computers, vol. 61, no. 2, pp. 187-198, Feb. 2012

• K. Stewart, Th. Haniotakis, and S. Tragoudas, Securing sensor networks: A novel approach that combines encoding, uncorrelation, and node disjoint transmission, Ad Hoc Networks, vol. 10, issue 3, May 2012, pp. 328-328, Elsevier.

• M.N. Skoufis, K. Karmakar, S. Tragoudas, and T. Haniotakis, A data capturing method for buses on chip, IEEE Transactions on Circuits and Systems I, vol. 57, no. 7, pp.1631-1641, July 2010.

• D. Jayaraman, R. Sethuram, and S. Tragoudas, Scan Shift Power Reduction by Gating Internal Nodes. J. Low Power Electronics 6(2): 311-319 (2010).

• E. Flanigan, S, Tragoudas, Path Delay Measurement Techniques using Linear Dependency Relationships, IEEE Transactions on VLSI Systems, vol. 18, issue 6, pp.1011-1015, June 2010.

• R. Adapa, S. Tragoudas, Techniques to Prioritize Paths for Diagnosis, IEEE Transactions on VLSI Systems, vol. 18, issue 4, pp. 658-661, April 2010.

• K. Christou, M. K. Michael, and S. Tragoudas, On the Use of ZBDDs for Implicit and Compact Critical Path Delay Fault Test Generation, Journal of Electronic Testing: Theory and Applications, 2008.

• A. Abdulrahman and S. Tragoudas, Low-Power Multi-Core ATPG to Target Concurrency, Integration, the VLSI Design Journal, vol. 41, issue 4, pp. 459-473, July 2008.

• C. Song, S. Tragoudas, Identification of Critical Executable Paths at the Architectural Level, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), vol. 27, no. 12, pp. 2291-2302, December 2008

I/UCRC Executive Summary - Project Synopsis		Date: 3/31/2014
Project Title: Comparison of Image Processing Algorithms on Micro-Array Architectures and GPGPU Platforms		
Center/Site: **Southern Illinois University Carbondale**		
Principle Investigator: Dr. Spyros Tragoudas		**Type: Continuing**
Tracking No.:	**Phone :** (618) 453 - 7027	**E-mail : spyros@engr.siu.edu**
		Proposed Budget: $25,000

Abstract:
The proposed project is a study analyzing the performance of image processing algorithms on General-Propose computing on Graphics Processing Units (GPGPU) architecture in comparison to a micro-core array embedded processor. The project will create a set of metrics which will measure speed, power consumption, and cost. Additionally, an investigation into the performance of several image processing algorithms such as a noise reduce, will be performed.

Problem:

- Currently no comprehensive survey comparing existing embedded systems processors to emerging mobile GPGPU platforms

Rationale / Approach:

- Focus shall be on implementation of image processing algorithms for in-house micro-core array processor and on GPGPU platforms with at least one mobile GPGPU platform.
- Optimizations shall be made to the set of image processing algorithms

Novelty:

- First Study to compare mobile versions of GPGPU the platform to current embedded systems
- Optimizations to existing Image Processing Algorithms will be made to better parallelize them

Potential Member Company Benefits:

- Member companies will gain additional insight into hardware platform trade-offs for future designs
- Gives better insight into implementation of image processing algorithms in embedded systems at a time when vision sensors are becoming commonplace.

Deliverables for the proposed year:

- Survey of GPGPU Platforms
- Comparison Study of the embedded system and GPGPU Platforms
- GPGPU Optimized Image Processing Algorithms

Milestones for the proposed year:

- Select GPGPU Platform (8/31/2014)
- Select a set of image processing algorithms (9/30/2014)
- Implement and optimize image processing algorithms on GPGPU platform (12/20/2014)
- Port algorithms to a multi-core embedded system (3/31/2015)
- Perform an Analysis on the performance difference between the platforms (7/31/2015)

Progress to Date:

- Acquired infrastructure for CUDA projects
- Previous experience in implementing parallel image processing algorithms

Estimated Start Date: 8/1/2014	**Estimated Knowledge Transfer Date**: 7/31/2015