Center for Embedded Systems (CES)
Request for Proposals Template – YEAR 6

DUE: Monday, March 31, 2014, by 5 p.m.

TITLE:	**Adaptive compressive sensing techniques for low power sensors**				
PI:	Haibo Wang and Spyros Tragoudas	**EMAIL:**	{haibo, Spyros}@engr.siu.edu	**TEL:**	618-453-1522 618-453-7645
DEPT:	ECE	**SCHOOL:**	Southern Illinois University		

ABSTRACT: (250 OR FEWER WORDS)

The objective of this project is to investigate novel adaptive approaches to more effectively apply compressive sensing (CS) techniques [1, 2] in low-power sensor systems. Recently, CS emerged as an attractive technique in low-power sensor development [3, 4, 5], because of its capability to allow sensor signals to be sampled at rates lowers than Nyquist rate. In CS operation, the number (denoted as M) of data points to be sensed or transmitted is selected according to the sparsity of the sensor signals. Currently, the majority of CS sensor circuits assume fixed M values during the entire sensing operations. To further reduce the power consumption of CS sensors, we have been investigating the potentials of adaptively adjusting the sampling rates in CS operations at system level. As a natural extension to the current effort, the proposed research is to investigate circuit techniques to execute adaptive compressive sensing at sensor nodes. Particularly, we will investigate the use of low-power analog wavelet transformation circuit to detect when sampling rate can be changed in adaptive CS operations.

PROBLEM:

The theory of CS operation is first briefly explained as follows. Assume vector X contains N sampled sensor outputs in time domain. Assume Ψ is *NXN* matrix that projects X into another domain by the relation of $X = \Psi \bullet \alpha$, where vector α contains the projected values and its size is also N. However, if α contains only K significant terms and the rest of N-K terms are zero or insignificant, sensor signal X is called sparse or compressible with respect to base Ψ (the sparseness refers to the value of K compared to N). For compressible signal X, CS operation produces compressed output Y using matrix operation $Y = \Phi \bullet X$, where Φ is an M×N matrix. Hence, Y is a vector with the size of M. For sensor signal X, if its corresponding α projection has only K significant terms, and Ψ and Φ are incoherent, the value of M that enables the receiver to reconstruct X from Y is $M = \mathrm{O}(K \log \frac{N}{K})$. If K<<N, then M<N, which implies that the sensor outputs can be potentially sampled at rates less than Nyquist rates. This makes CS technology extremely attractive to low-power sensor design.

The above discussion indicates that the measurement size M in CS operation is affected by signal sparsity, which may vary over the time. Hence, it is naturally expected that the CS measurement size, or sampling rate, should follow the variations of signal sparsity. We refer to the CS operations, in which the sampling rates are adaptively adjusted according to the signal sparsity variations, as adaptive compressive sensing (ACS). At present, the sampling rates (or measurement size) in the CS operations of these low-power sensors are fixed according to prior knowledge of signal sparsity [3, 4, 5], and hence do not change during sensing operations. In related studies, the work [6] exploits signal sparsity variations to dynamically adjust sampling rate. It targets image applications and does not investigate the potential power saving by ACS. The approach in [7] adaptively adjusts the coefficients in the mathematic basis that are used in the reconstruction of the signal. It does not change the sampling rate at the sensing end.

RATIONALE:

The need for ACS operation depends on whether signal sparsity significantly varies over the time, which is strongly application dependent. In the early phase of the project, we examined a larger number of real biomedical sensor signals collected from the Multiparameter Intelligent Monitoring in Intensive Care (MIMIC II) database [8] to study the sparsity variations of these signals as well as the required CS measurement sizes at different time periods. It shows that the sparsity characteristics and the required measurement sizes of many biomedical sensor signals do vary over the time as shown in Figure 1, and hence it is possible to perform ACS for such signals [9].

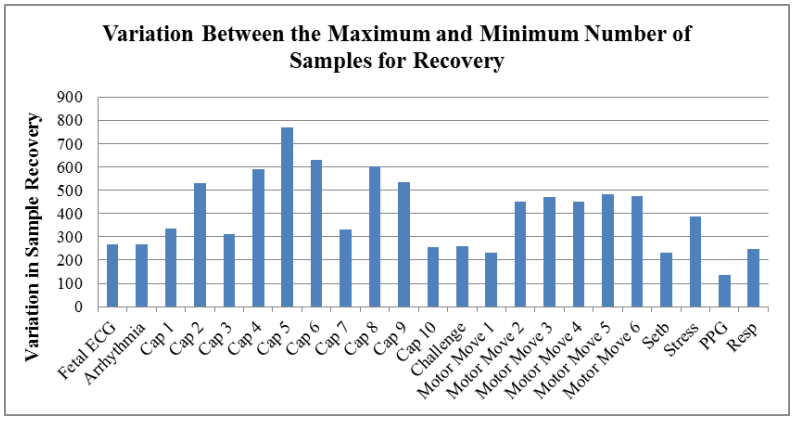

Fig. 1: Variation between the maximum and minimum number of samples.

Table 1. Potential Power Saving by ACS

Signal	Conv. CS	ACS	Power Savings
Fetal ECG	3.08 mW	2.31 mW	25%
Cap	4.57 mW	3.75 mW	17.2%
Stress	2.98 mW	1.57 mW	47.3%
PPG	1.55 mW	1.27 mW	18.1%

The early phase of the project also investigated the potential power savings by applying ACS in wireless sensors. The study assumes that the power consumption of the wireless transmitter dominates the overall power consumption of the sensor node, which is true for most wireless sensors [4]. A generic power model is used to estimate the power consumption of the transmitter along with the signal sparsity characteristics. As shown in Table 1, the results demonstrate significant power savings using ACS techniques, compared to conventional CS techniques [9]. Motivated by these findings, the proposed project investigates techniques for implementing the proposed ACS techniques in the design of low-power sensors.

APPROACH:

An import question that needs to be answered in the implementation of ACS techniques is how to detect signal sparsity variations and subsequently adjust the sampling rate. In the project, we propose to use a low-power analog (continuous-time) wavelet transformation (WT) circuit to monitor the signal sparsity during sensor operation and to adjust the sampling rates according to the output of the analog WT circuit. We will first develop analog WT circuits, and then experimentally (via simulation) establish the relation between the analog WT circuit output and the signal sparsity as shown in Figure 2. Extensive simulations will be performed to investigate the performance of the proposed approach.

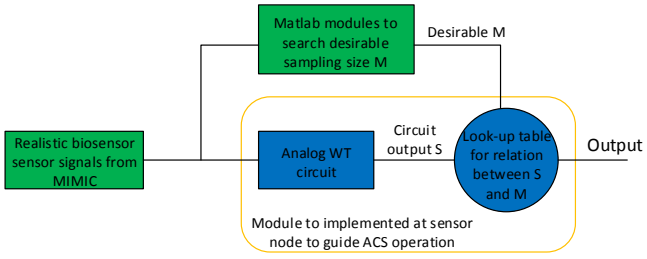

Fig. 2: Establishing the relation between signal sparsity and the output of analog WT circuits

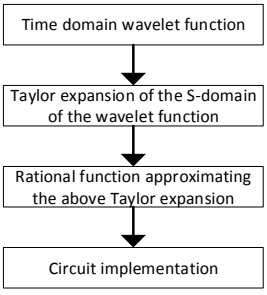

Fig. 3: Design flow for developing analog WT circuits

The design flow for the analog WT circuit is illustrated in Figure 3. First, we select proper wavelet functions based on signal sparsity analysis and simulation. Then the Laplace domain expression of the selected wavelet function is obtained and expanded into the Taylor series format. The Taylor expression is fed to a Pade approximation package to obtain a rational expression (transfer function) that approximates the original Laplace domain expression. Finally, the circuit implementation can be derived from the obtained transfer function. The circuit will be developed based on gm-C circuit techniques and implemented using a 0.13μ CMOS technology.

NOVELTY:

CS is a relatively new approach to reduce the power consumption of certain type sensors. The proposed work helps make CS sensors more power efficient, hence advances the state of the art of CS sensor techniques.

POTENTIAL BENEFITS TO INDUSTRY MEMBERS:

The developed techniques have the potentials to help member companies further reduce the power consumptions of certain sensor devices in productions, or to be used in their research and development (R&D) projects.

DELIVERABLES:

1. Design of the analog wavelet transformation circuits
2. Investigation results on the effectiveness of using analog wavelet transformation circuit to determine the sampling rates in ACS operations

TIMELINE/MILESTONES: (PER QUARTER)

1. **Quarter 1 (08/14-10/14):** Select a set of wavelet functions to be implemented
2. **Quarter 2 (11/14-01/15):** Obtain stable transfer function and start analog WT circuit development work
3. **Quarter 3 (02/15-04/15):** Complete the development of analog WT circuits
4. **Quarter 4 (05/15-07/15):** Establish the relation between analog WT circuit output and signal sparsity; investigate the effectiveness of the proposed approach

TECHNOLOGY TRANSFER:

1. Low-power circuit techniques for implementing continuous-time wavelet transformation circuits
2. Knowledge on using continuous-time wavelet transformation circuit to monitor signal sparsity and subsequently determine optimal sampling rate for adaptive compressive sensing

BUDGET:

The requested budget is $50,000. Among them, $29,952 is to support PhD students (1 student @50% for 12 months, 1 student @25% for 12 months) and $20,048 is for the salaries of the two PIs and travel. ***SIUC match: $41,300*** ($23,750 on indirect cost waiver and $17550 on PhD student tuition waiver)

BIBLIOGRAPHY: (ATTACH IN IEEE CONFERENCE OR JOURNAL FORMAT)

1. D. Donoho, "Compressed sensing," IEEE Transactions on Biomedical Engineering, Vol. 52, No. 4, pp. 1289–1306, April 2006.
2. E. Candes, J. Romberg, and T. Tao, "Stable signal recovery from incomplete and inaccurate measurements," Communications on Pure and Applied Mathematics, Vol. 59, No. 8, pp. 1207–1223, August 2006.
3. Allstot, E.G.; Chen, A.Y.; Dixon, A.M.R.; Gangopadhyay, D.; Allstot, D.J.; "Compressive sampling of ECG bio-signals: Quantization noise and sparsity considerations," 2010 IEEE Biomedical Circuits and Systems Conference (BioCAS), pp. 41-44, Nov. 2010.
4. Chen, F.; Chandrakasan, A.P.; Stojanovic, V.; "A Signal-agnostic Compressed Sensing Acquisition System for Wireless and Implantable Sensors," 2010 IEEE Custom Integrated Circuits Conference (CICC), pp. 1-4, Sept. 2010.
5. Baheti, P.K.; Garudadri, H.; "An ultra-low power pulse oximeter sensor based on compressed sensing," Sixth International Workshop on Wearable and Implantable Body Sensor Networks, pp. 144-148, 2009.
6. Warnell, G., Reddy, D., and Chellappa, R. Adaptive rate compressive sensing for background subtraction. 2012 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), (2012), 1477–1480.
7. Soni, A. and Haupt, J. Efficient adaptive compressive sensing using sparse hierarchical learned dictionaries. 2011 Conference Record of the Forty Fifth Asilomar Conference on Signals, Systems and Computers (ASILOMAR), (2011), 1250–1254.
8. Saeed, M., Villarroel, M., Reisner, A.T., et al. Multiparameter Intelligent Monitoring in Intensive Care II (MIMIC-II): A public-access intensive care unit database. Critical care medicine 39, 5 (2011), 952–960.
9. Adam Watkins, Venkata Naresh Mudhireddy, Haibo Wang and Spyros Tragoudas, "Adaptive Compressive Sensing for Low Power Wireless Sensors," accepted by GLSVLSI, 2014, May 2014

PI INFORMATION: (ATTACH 2-PAGE CV)

BIOGRAPHICAL SKETCH

Haibo Wang
Department of Electrical and Computer Engineering
Southern Illinois University, Carbondale, IL 62901-6603
Phone: (618) 453-1522; E-mail: zhwang@siu.edu

Professional Preparation:

University of Arizona, Tucson	Ph.D.	Electrical and Comp. Engineering	5/02
Nanyang Technological Univ., Singapore	M. Eng.	Electrical Engineering	4/97
Tsinghua University, Beijing, China	B. Eng.	Electronic Engineering	7/92

Professional Experience:

7/13 – present	Professor, Department of Electrical and Computer Engineering, Southern Illinois University (SIU), Carbondale, IL 62901
7/07 – 6/13	Associate Professor, Department of Electrical and Computer Engineering, Southern Illinois University (SIU), Carbondale, IL 62901
8/02 – 6/07	Assistant Professor, Department of Electrical and Computer Engineering, Southern Illinois University (SIU), Carbondale, IL 62901
1/97 – 5/02	Research Assistant, Department of Electrical and Computer Engineering, University of Arizona, Tucson, AZ 85721
5/00 – 8/00	Intern, Wireless Integration Technology Center, Motorola, Libertyville, IL 60030
6/98 – 8/98	Intern, Rockwell Semiconductor Systems, San Diego, CA 92121
9/96 – 12/96	IC Design Engineer, Siemens Components Pte. Ltd., Singapore, 349249
9/94 – 8/96	Research Assistant, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, 639798
9/92 – 8/94	Teaching Assistant, Institute of Microelectronics, Tsinghua University, Beijing, China

Honors and Awards:

- NSF CAREER award, 2005
- Best paper award, 8th International Symposium on Quality Electronic Design, San Jose, CA, 2007
- Outstanding paper award, 8th International Conference on Mixed Design of Integrated Circuits and Systems, Poland, 2001

Research Funding:

- I/UCRC: Collaborative Research: Synthesis and Design of Robust Threshold Logic Circuits, NSF, PI: Spyros Tragoudas, Co-PI: Haibo Wang, $100,000, 08/12-07/14
- Adaptive Compressive Sensing Techniques for ultra-low power sensors, NSF IUCRC, PI: Haibo Wang, Co-PI: Spyros Tragoudas, $50,000, 08/12-07/13
- In-plant Demonstration of a Low-cost Automation System for Coal Spiral, Illinois Department of Commerce and Economic Opportunity (IDCEO/ICCI), PI: Manoj Mohanty, Co-PI: Haibo Wang, $164,993, 02/12-07/13
- Development of Telemetry Circuit for Sol-gel Sensors, NSF IUCRC Center for Embedded Systems, PI: Haibo Wang, Phase I: $25,000, 09/09-08/10, Phase II 25,000, 09/10-08/11
- Development and demonstration of an automation and control system for coal spiral, Illinois Department of Commerce and Economic Opportunity (IDCEO/ICCI), PI: Manoj Mohanty, Co-PI: Haibo Wang, $149,897, 01/10-05/11
- CAREER: implementing mixed-signal circuits with self-testing and self-repairing capabilities, NSF, PI: Haibo Wang, $400,000, 03/05–02/10
- A Portable Medical Instrument for Objectively Diagnosing Human Tinnitus, SIU School of Medicine, Concept Development Award, PI: Jeremy Turner, Co-PI's: Jun Qin, Haibo Wang, $13,800, 08/09-05/10

- An Ultrasonic Tracking System for Motion Capture Studies in Ergonomic Applications, Caterpillar, Inc., PI: Ajay Mahajan, co-PI: Haibo Wang, Phase I: $39,995, 05/06-08/07; Phase II: $75,720, 09/07-12/08; Phase III: $95,031, 12/08-12/09

Professional Service:

- Technical Program Committee of 24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2009, Chicago, IL.
- Technical Program Committee of 2007-2012 International Symposium of Quality Electronic Design, San Jose, CA.
- Session Co-Chairs at 2007, 2008 International Symposium of Quality Electronic Design, San Jose, CA.
- Program Committee of 2003 International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland
- Session Chair of 2000 International Symposium on Circuits and Systems, Phoenix AZ.

Selected Publications:

1. Mallik Kandala and Haibo Wang, "a 0.5V High-speed comparator with rail-to-rail input range," Analog Integrated Circuits and Signal Processing, Vol. 73, No. 1, pp.415-421, September, 2012
2. Chenglong Zhang and Haibo Wang, "Reeducation of Parasitic Capacitance impact in low-power SAR ADC," , *IEEE Transactions on Instrumentation and Measurement*, Vol.61, No.3, pp.587-594, March 2012
3. Yongtao Geng, Huan Zou, Chaojiang Li, Jiwei Sun, Haibo Wang and Pingshan Wang, "Short Pulse Generation With On-Chip Pulse-Forming Lines," IEEE trans. on VLSI, Vol. 20, No. 9, pp. 1553-1564, September 2012
4. Pingshan Wang, Haibo Wang, Yueran Gao, Yongtao Geng and George Thomas, "A High-Speed Sample-and-hold Circuit Based on CMOS Transmission Lines," Analog Integrated Circuits and Signal Processing, Vol. 66, No. 2, pp245-254, February, 2011
5. B. Soewito, L. Vespa, N. Weng, and H. Wang, "Hybrid pattern matching for trusted intrusion detection," Security and Communication Networks, Vol. 4, No. 1, pp. 33-43, January, 2011
6. Mallik Kandala and Haibo Wang, "Low-power Circuit Techniques for Successive Approximation Register ADC Design," Journal of Low-Power Electronics, Vol. 6, No. 2, pp.300-310, August, 2010.
7. Huan Zou, Hanqiao Zhang, Chunrong Song, Haibo Wang, Pingshan Wang, "Characterization and modeling of mitered coplanar waveguide bends on silicon substrates," International Journal of Electronics, Vol. 97, No. 6, pp. 715-727, October 2010.
8. B. Soewito, L. Vespa, A. Mahajan, N. Weng and H. Wang, "Self Addressable Memory-based FSM (SAM-FSM): A Scalable Intrusion Detection Engine," IEEE Network, vo. 23, no. 1, pp. 14 - 21, January, 2009
9. B. Soewito, A. Mahajan, N. Weng, and H. Wang, "High-speed String Matching for Network Intrusion Detection," Int. Journal of Communication Networks and Distributed Systems (IJCNDS), Vol. 3, No. 4, pp. 319-339, 2009.
10. A. Laknaur, R. Xiao, S. Durbha, and H. Wang, "Design of a Window Comparator with Adaptive Error Threshold for Online Testing Applications," Microelectronics Journal, Vol. 40, No. 9, pp. 1257-1263, 2009.

SPYROS TRAGOUDAS

PROFESSIONAL AFFILIATION AND CONTACT INFORMATION

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EDUCATION

1986 Diploma (5 years), Computer Engineering and Informatics Department, University of Patras, Greece

1988 M.S., Erik Jonsson School of Engineering and Computer Science, Computer Science Program, The University of Texas at Dallas, Richardson, TX 75083-0688.

1991 Ph.D., Erik Johnson School of Engineering and Computer Science, Computer Science Program, The University of Texas at Dallas, Richardson, TX 75083-0688.

PROFESSIONAL EXPERIENCE

07/1/12- current Department Chair, Electrical & Computer Eng. Dept., Southern Illinois University Carbondale.

03/01/09-current Director, NSF IUCRC on Embedded Systems, SIUC-site.

07/16/99- current Professor, Electrical & Computer Eng. Dept., Southern Illinois University Carbondale.

08/16/98-07/15/99 Associate Professor, Electrical and Computer Engineering Department, The University of Arizona.

08/16/91-08/15/98 Associate Professor, Computer Science Department, Southern Illinois University Carbondale (in the rank of untenured Assistant Professor until 6/30/96).

07/01/97-08/15/98 Graduate Program Director, Computer Science Department, Southern Illinois University Carbondale.

01/03/87-08/14/91 Research/Teaching Assistant, Computer Science Program, School of Engineering and Computer Science, The University of Texas at Dallas, Richardson, TX 75083-0688.

08/15/86-01/02/87 Systems Analyst, Computer Technology Institute, Patras, Greece.

RESEARCH INTERESTS

Design and Test Automation for VLSI, Embedded Systems

RESEARCH SPONSORS

Direct support: National Science Foundation, US Navy, SAIC, Intel, Qualcomm, Synopsys

NSF IUCRC: NSF, NAVSEA Crane, SAIC, Intel, Caterpillar, Dickey-john, EMAC, Wildlife Materials

PROFESSIONAL SERVICE

Editorial Board: IEEE Transactions on Computers, VLSI Design journal, Universal Computer Science, Research Letters in Electronics.

General Chair of IEEE DFTS 2010, Program Committee Chair of DFTS 2009, Program Committee member of many International Conferences

Has graduated 14 PhD students and supervised over 60 MS theses. Currently advising 11 PhD students

PUBLICATIONS

Over 60 journal papers and over 100 articles in peer-reviewed conference proceedings

Ten recent journal publications

• A.K. Palaniswamy and S.Tragoudas, An Efficient Heuristic to Identify Threshold Logic Functions, ACM Journal on Emerging Technologies in Computing (JETC), to appear in 2012.

• M.N. Skoufis, S. Tragoudas, An on-line Failure Detection Method for Data Buses using Multi-threshold Receiving Logic, IEEE Transactions on Computers, vol. 61, no. 2, pp. 187-198, Feb. 2012

• K. Stewart, Th. Haniotakis, and S. Tragoudas, Securing sensor networks: A novel approach that combines encoding, uncorrelation, and node disjoint transmission, Ad Hoc Networks, vol. 10, issue 3, May 2012, pp. 328-328, Elsevier.

• M.N. Skoufis, K. Karmakar, S. Tragoudas, and T. Haniotakis, A data capturing method for buses on chip, IEEE Transactions on Circuits and Systems I, vol. 57, no. 7, pp.1631-1641, July 2010.

• D. Jayaraman, R. Sethuram, and S. Tragoudas, Scan Shift Power Reduction by Gating Internal Nodes. J. Low Power Electronics 6(2): 311-319 (2010).

• E. Flanigan, S, Tragoudas, Path Delay Measurement Techniques using Linear Dependency Relationships, IEEE Transactions on VLSI Systems, vol. 18, issue 6, pp.1011-1015, June 2010.

• R. Adapa, S. Tragoudas, Techniques to Prioritize Paths for Diagnosis, IEEE Transactions on VLSI Systems, vol. 18, issue 4, pp. 658-661, April 2010.

• K. Christou, M. K. Michael, and S. Tragoudas, On the Use of ZBDDs for Implicit and Compact Critical Path Delay Fault Test Generation, Journal of Electronic Testing: Theory and Applications, 2008.

• A. Abdulrahman and S. Tragoudas, Low-Power Multi-Core ATPG to Target Concurrency, Integration, the VLSI Design Journal, vol. 41, issue 4, pp. 459-473, July 2008.

• C. Song, S. Tragoudas, Identification of Critical Executable Paths at the Architectural Level, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), vol. 27, no. 12, pp. 2291-2302, December 2008.

I/UCRC Executive Summary - Project Synopsis		Date: 3/31/2014
Project Title: Adaptive compressive sensing techniques for low power sensors		
Center/Site: Center for Embedded Systems/Southern Illinois University		
Principle Investigator: Haibo Wang and Spyros Tragoudas		**Type: (New or Continuing)** Continuing
Tracking No.: (CES office to input)	**Phone :** (618) 453 - 1522 (618) 453 - 7645	**E-mail :** {haibo, Spyros}@engr.siu.edu
		Proposed Budget: $50,000

Abstract: (250 words max)
The objective of this project is to investigate novel adaptive approaches to more effectively apply compressive sensing (CS) techniques in low-power sensor systems. Recently, CS emerged as an attractive technique in low-power sensor development because of its capability to allow sensor signals to be sampled at rates lowers than Nyquist rate. To further reduce the power consumption of CS sensors, we have been investigating the potentials of adaptively adjusting the sampling rates used in CS operations at system level. As a natural extension to the current effort, the proposed research is to investigate circuit techniques to execute adaptive CS operation at sensor nodes. Particularly, we will investigate the use of low-power analog wavelet transformation circuit to detect when sampling rate can be changed in adaptive CS operation.

Problem:
In CS operation, the measurement size (or sampling rate) is affected by signal sparsity, which may vary over the time. Hence, it is naturally expected that the CS measurement size (or sampling rate), should follow the variations of signal sparsity. Such CS operation is called adaptive CS (ACS). At present, the sampling rates of the reported CS sensors are fixed according to prior knowledge of signal sparsity, and hence do not change during sensing operations. By exploiting signal sparsity variations, ACS can potentially lead to further power reduction in low-power sensors.

Rationale / Approach:
The findings in the early phase of the project indicate that there are significant signal sparsity variation over the time and applying ACS potentially lead to significant power saving. The proposed work intends to develop techniques to detect the signal sparsity variations and subsequently adjust the sampling rate. We propose to use a low-power analog (continuous-time) wavelet transformation (WT) circuit to monitor the signal sparsity during sensor operation and to adjust the sampling rates according to the output of the analog WT circuit.

Novelty:
CS is a relatively new approach to reduce the power consumption of certain type sensors. The proposed work helps make CS sensors more power efficient, hence advances the state of the art of CS sensors.

Potential Member Company Benefits:
The developed techniques have the potentials to help member companies further reduce the power consumptions of certain sensor devices in productions or to be used in their research and development (R&D) projects.

Deliverables for the proposed year:
1. Design of the analog wavelet transformation circuit
2. Investigation results on the effectiveness of using analog wavelet transformation circuit to determine the sampling rates in adaptive compressive sensing

Milestones for the proposed year:
1. **Quarter 1 (08/14-10/14):** Select a set of wavelet functions to be implemented
2. **Quarter 2 (11/14-01/15):** Obtain stable transfer function and start analog WT circuit development work
3. **Quarter 3 (02/15-04/15):** Complete the development of analog WT circuits
4. **Quarter 4 (05/15-07/15):** Establish the relation between analog WT circuit output and signal sparsity

Progress to Date: **THIS SECTION TO BE UPDATED IN JANUARY**

Estimated Start Date: 8/18/2014	**Estimated Knowledge Transfer Date**:7/31/2015