Center for Embedded Systems

An NSF Industry/University Cooperative Research Center

Towards Predictable Execution of Safety-Critical Tasks on Mixed-Criticality Multi-Core Platforms

PIs:

Harini Ramaprasad

Dimitri Kagaris

Southern Illinois University Carbondale

SIU Southern Illinois University Carbondale

National Science Foundation

ASU Ira A. Fulton Schools of Engineering Arizona State University

Project Overview and Description

- **Problem**
  - Deterministic execution of HSS tasks in presence of LSS ones on multi-core architectures is challenging.
- **Viable Solution**
  - Virtualization (hypervisor) for isolation of HSS & LSS task sets
  - Cache-locking and partitioning for improved predictability
- **Applications**
  - Integrate multiple avionics modules in single box
- **Project Description**
  - Conduct trade-off study of *determinism* vs *performance* of mixed-criticality tasks on Freescale P4080 multi-core platform
  - Develop policies to maintain responsiveness of HSS applications under regular and overload conditions

Approach

- **Two stages**
  - **Stage 1**: a) Use cache locking and partitioning to improve predictability of HSS tasks; b) Identify/develop suitable policies to apply to end-user scenarios.
  - **Stage 2**: Explore the use of manager partition to dynamically control resource usage of LSS tasks under overload or unexpected situations
- **Metrics** for measuring success of techniques
  - HSS tasks: determinism (satisfaction of timing and precedence constraints
  - LSS tasks: Quality-of-Service (QoS)
- **Benefit to member companies**
  - Integration on Multicore → save space and cost
  - Use of hypervisor → Safe execution of mixed-criticality workloads

Project Tasks/ Deliverables

	Description	Date	Status
1	Exploration of existing research in the area of cache locking and partitioning.	Q1	Not yet started
2	Workload characterization and end-use scenario analysis under cache locking and partitioning schemes.	Q2	Not yet started
3	Exploration of mechanisms to create and configure manager partitions;	Q3	Not yet started
4	Development of strategies for dynamic resource management using manager partitions	Q3	Not yet started
5	Report writing and technology transfer	Q4	Not yet started

Technical Detail

- **Freescale QorIQ P4080**
  - 8 high-performance cores
  - Private L1 & L2, shared L3
  - Embedded hypervisor
    - •Provides support for safe *partitioning* of cores, memory, I/O devices
    - •Can configure one partition as *"manager partition"*
  - High-bandwidth communication & coherence infrastructure
    - •Support for prioritization, bandwidth allocation, packet-level queue management and QoS scheduling
  - Hypervisor design
    - •Exploits hardware mechanisms in cores to improve efficiency of virtualization
    - •Easier to bound hypervisor interference across OSs