Center for Embedded Systems

An NSF Industry/University Cooperative Research Center

Towards Predictable Execution of Safety-Critical Tasks on Mixed-Criticality Multi-Core Platforms

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Project Overview and Description

- **Motivation**
  - Multi-core architectures→high performance, low power
- **Problem**
  - Deterministic execution of highly safety-sensitive (HSS) tasks in presence of less safety-sensitive (LSS) ones is challenging due to shared resources
- **Viable Solution**
  - Virtualization (hypervisor) for isolation of HSS & LSS task sets
- **Project Description**
  - Comprehensive trade-off study of *determinism* vs *performance* of mixed-criticality tasks executing in the Freescale P4080 multi-core platform

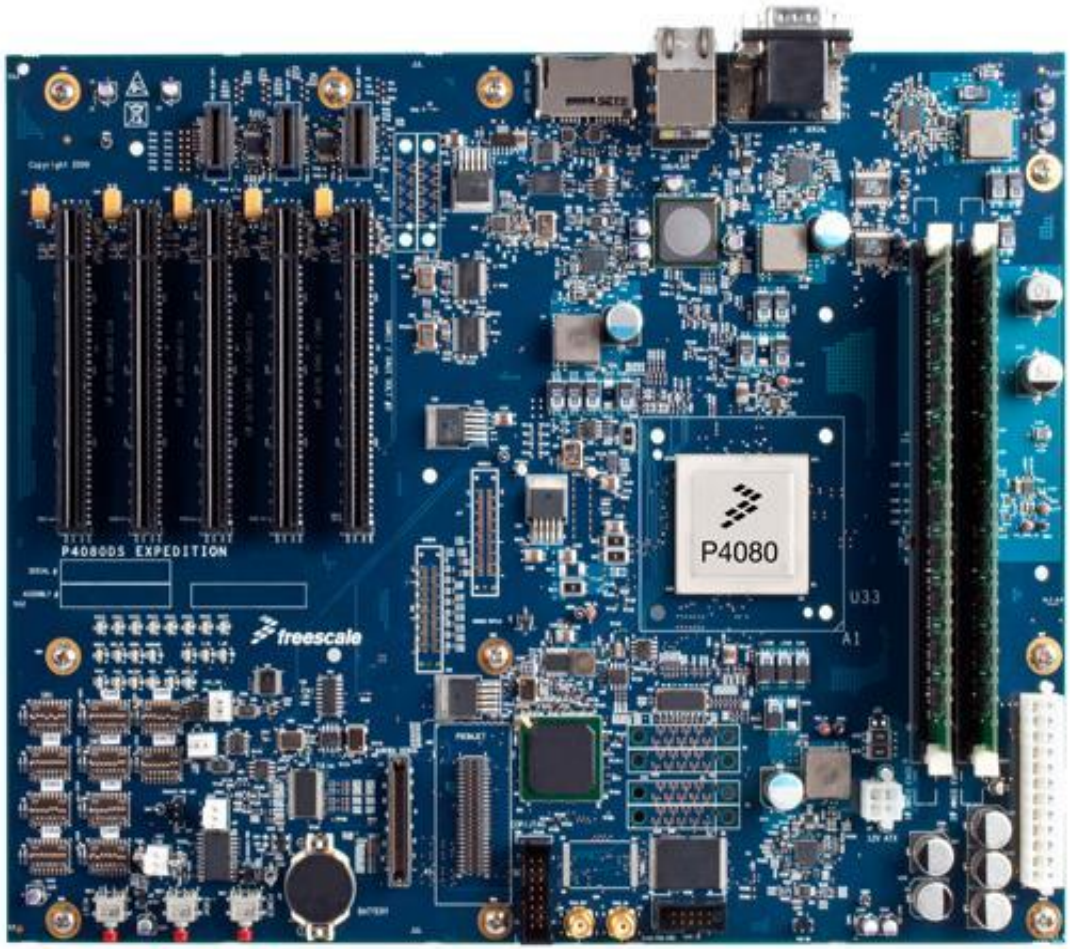
Approach

- Explore time and space partitioning of resources among task sets executing within real-time and general-purpose operating systems
- Develop heuristics for time-efficient solutions
- Employ a two-stage approach
  - **Stage 1:** aggregate requirements of tasks within each OS and study determinism and responsiveness across OSs
  - **Stage 2:** study determinism and responsiveness of individual tasks within each OS
- Metrics for measuring success of resource allocation
  - HSS tasks: determinism of execution (satisfaction of timing and precedence constraints
  - LSS tasks: Quality-of-Service (QoS)

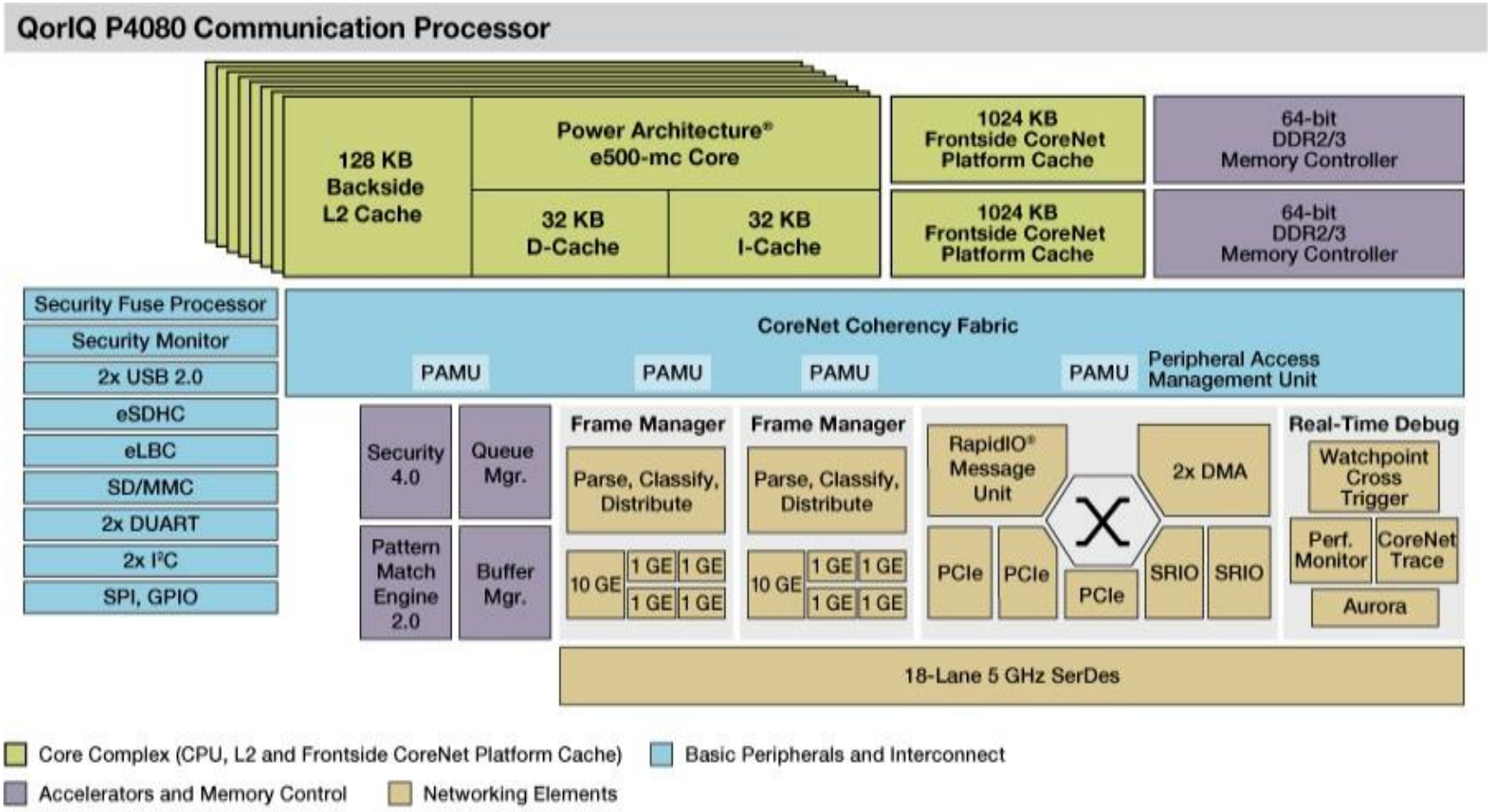
Experimental platform → ***Freescale QorIQ P4080***

P4080 Development System

P4080



Picture from: 2004-2013 Freescale Semiconductor, Inc.


QorIQ P4080 Communication Processor
128 KB Backside L2 Cache
Power Architecture® e500-mc Core
32 KB D-Cache
32 KB I-Cache
1024 KB Frontside CoreNet Platform Cache
1024 KB Frontside CoreNet Platform Cache
64-bit DDR2/3 Memory Controller
64-bit DDR2/3 Memory Controller
Security Fuse Processor
Security Monitor
2x USB 2.0
eSDHC
eLBC
SD/MMC
2x DUART
2x I²C
SPI, GPIO
CoreNet Coherency Fabric
PAMU
PAMU
PAMU
PAMU
Peripheral Access Management Unit
Security 4.0
Queue Mgr.
Pattern Match Engine 2.0
Buffer Mgr.
Frame Manager
Parse, Classify, Distribute
10 GE
1 GE
1 GE
1 GE
1 GE
Frame Manager
Parse, Classify, Distribute
10 GE
1 GE
1 GE
1 GE
1 GE
RapidIO® Message Unit
2x DMA
PCIe
PCIe
PCIe
SRIO
SRIO
Real-Time Debug
Watchpoint Cross Trigger
Perf. Monitor
CoreNet Trace
Aurora
18-Lane 5 GHz SerDes
Core Complex (CPU, L2 and Frontside CoreNet Platform Cache)
Basic Peripherals and Interconnect
Accelerators and Memory Control
Networking Elements

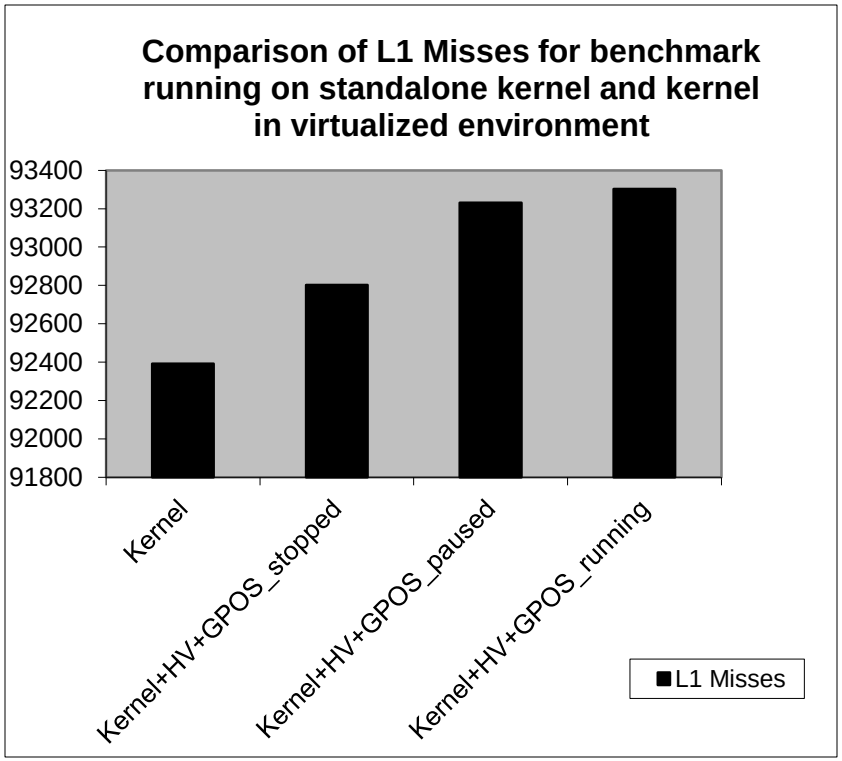
Technical Detail

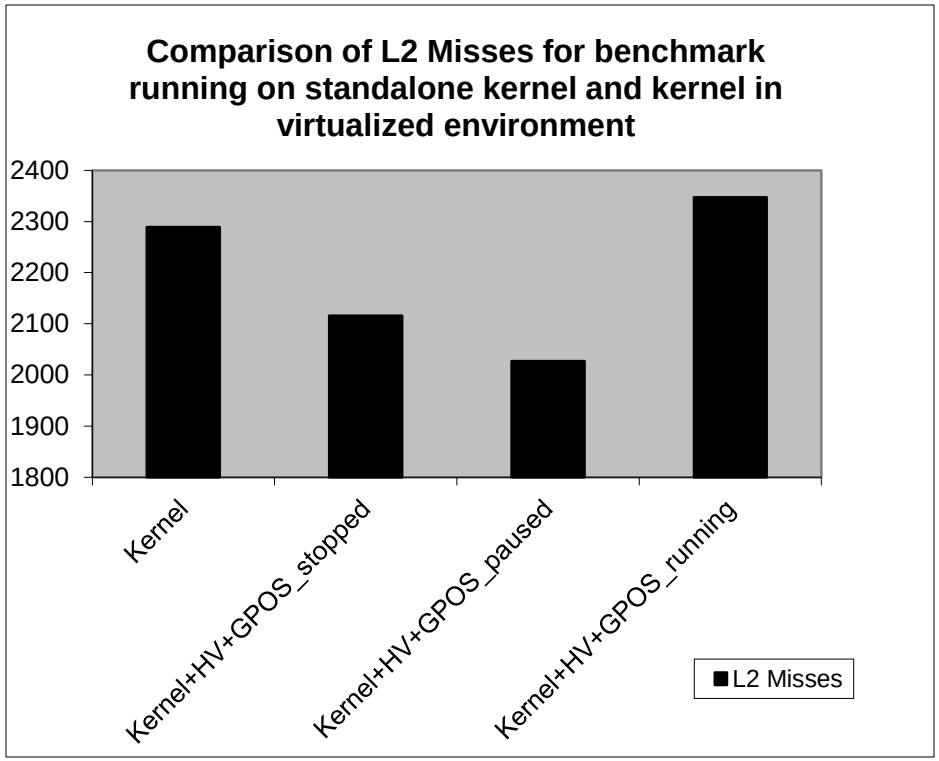
- **Freescale QorIQ P4080**
  - 8 high-performance cores with private L1, L2 and shared L3.
  - Embedded hypervisor
    - Safe OS partitioning and support for partitioning cores, memory and I/O devices.
  - High-bandwidth communication & coherence infrastructure
  - Support for prioritization, bandwidth allocation, packet-level queue management and QoS scheduling
  - Suitability of Freescale P4080 platform
    - Scheduling granularity is coarse which allows static partitioning of resources. Suitable for systems with HSS tasks where determinism is paramount
    - Hypervisor design exploits hardware mechanisms in cores to improve efficiency of virtualization. Easier to bound hypervisor interference across OSs
  - Benchmarks for creation of mixed-criticality task sets
    - MRTC WCET benchmarks
    - EEMBC benchmarks: LMBench, CoreMark, perf_measure(RCI)

RT Performance comparison between Virtualized and non-Virtualized mode

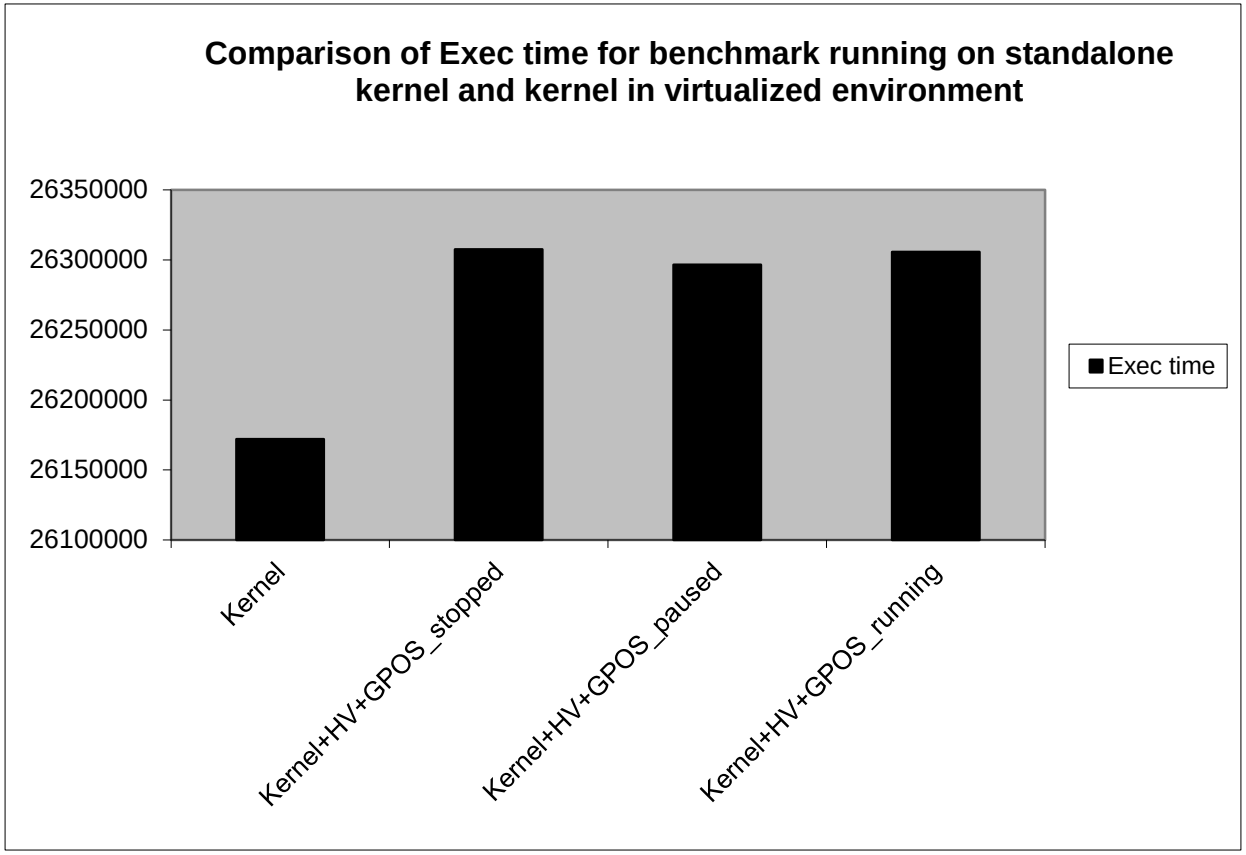
- Study overheads due to the presence of hypervisor
  - Execute on standalone kernel and virtualized kernel
  - Study L1, L2 behavior and task execution times
- Study performance of tasks on RT partition
  - Execute HSS tasks in RT partition
  - Vary memory usage in GP partition and study effects on tasks in RT partition

L1 and L2 cache misses

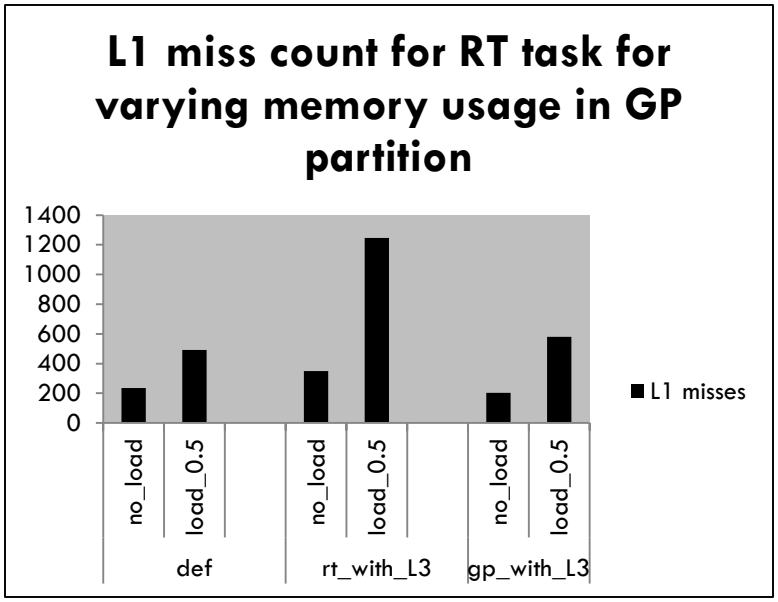


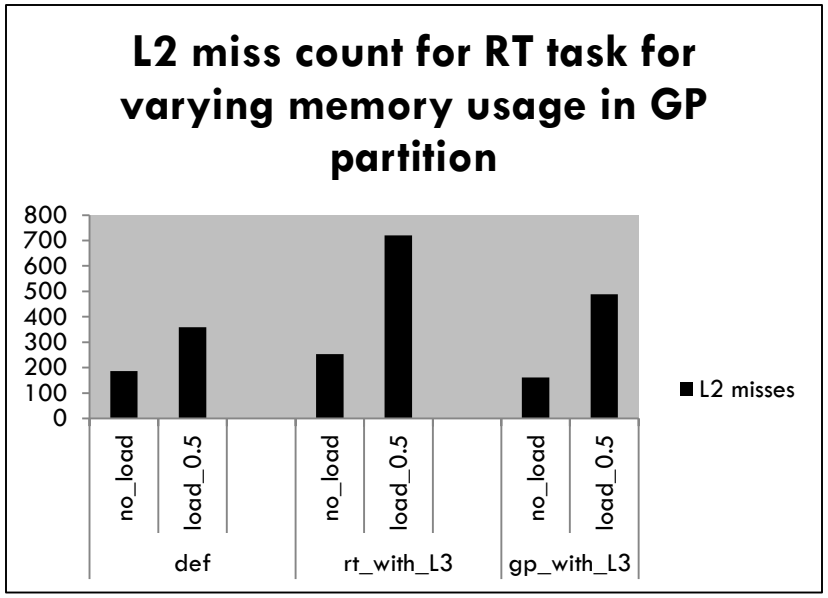


Execution time

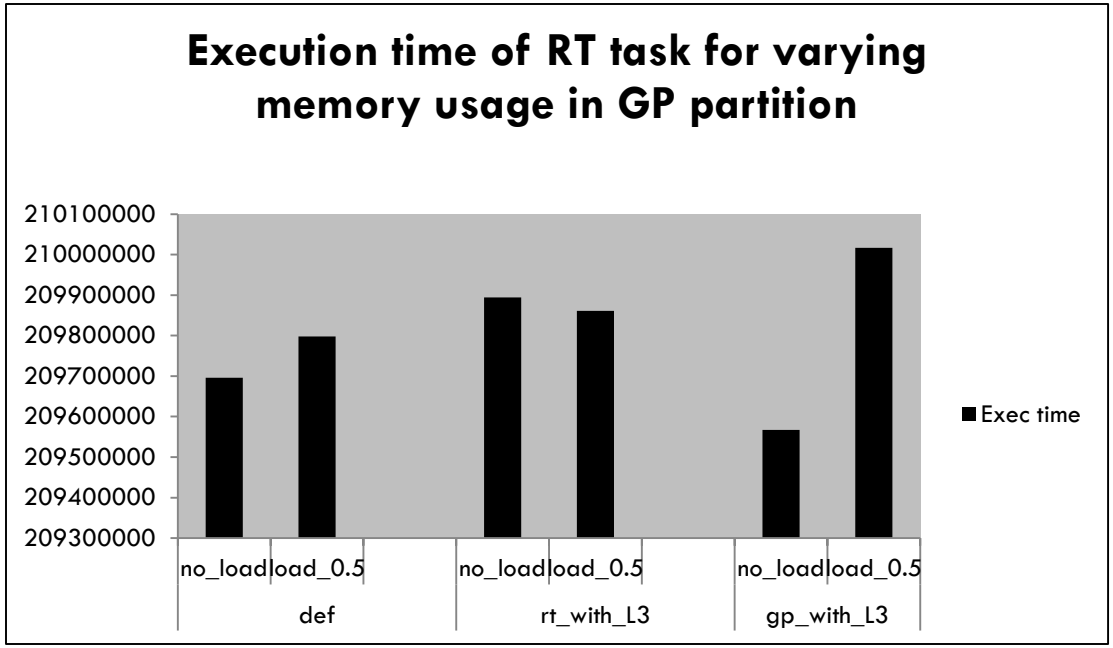


L1 and L2 cache misses for varying memory usage in GP partition





Execution time of RT task for varying memory usage in GP partition



Observations

- Problems
  - Hypervisor allows multiple partitions, but adds overhead
  - Execution time of tasks on RT partition (HSS tasks)
    - Increases when there is memory load on GP partition
    - Is sometimes inconsistent across multiple runs
- Potential solutions
  - Lock cache lines tasks on RT partition to improve predictability
  - Partition cache among guest RT & GP OSs to improve determinism and responsiveness of tasks on RT partition

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