Mid-term Update Process

Presenter

- Each presenter will have 3 minutes for their short “elevator pitch”
- Each presenter has a poster setup in the back of the room to use for deep-dive discussions with the industry members
- Five or Six presentations back-to-back
- Immediately following the presentations is a 90 minutes for industry members to interact with all presenters

Industry Members

- Please hold questions for poster sessions
- Please show your appreciation to the presenters when the timer elapses by applauding 
- During poster session, please rotate to all presenters posters when asked to do so

Host

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- During the 90 minute poster session, the host will notify industry members when it is time to “rotate to next poster”

Center for Embedded Systems

An NSF Industry/University Cooperative Research Center

YEAR 5: IAB Mid-term Update

Sarma Vrudhula, Professor
Arizona State University

Spyros Tragoudas, Professor
Southern Illinois University - Carbondale

SIU Southern Illinois University CARBONDALE

NATIONAL SCIENCE FOUNDATION

ASU Ira A. Fulton Schools of Engineering
ARIZONA STATE UNIVERSITY

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Group 1

1.1:	S4.Y5.ST	Multicore Simulator Critical Path Analysis	Spyros Tragoudas	SIU
1.2:	A8.Y5.HB	Readout Integrated Circuit for Fast Imager	Hugh Barnaby	ASU
1.3:	S1.Y5.CH	Ground Work for Embedding a Field Oriented Motor Controller into a Single System on a Chip	Constantine Hatziadoniu	SIU
1.4:	A9.Y5.KSC	I2AV: Integrate, Index, Analyze, and Visualize Energy Data for Data-driven Simulations and Optimizations	K. Selcuk Candan	ASU
1.5:	S3.Y5.ST	An Effective Test Strategy Based on Coverage Driven ATPG	Spyros Tragoudas & Themistoklis Haniotakis	SIU
1.6:	A1.Y5.GF.YK	Visual Interface for Metric Temporal Logic Specifications	Georgios Fainekos, Yoshihiro Kobayashi	ASU

Group 2

2.1:	**A7.Y5.CW**	Achieving Energy-efficient Mobile Computing Through Explicit Data Communication and Global Power Management	Carole-Jean Wu	ASU
2.2:	S5.Y5.HR.DK	Towards Predictable Execution of Safety-Critical Tasks on Mixed-Criticality Multi-Core Platforms	Harini Ramaprasad, Dimitrios Kagaris	SIU
2.3:	A2.Y5.GF.YHL	Parallelization of Embedded Control Applications on Multi-core Architectures: A Case Study	Georgios Fainekos, Yann-Hang Lee	ASU
2.4	JOINT.Y5.ST.SV.HW.FRP	Synthesis and Design of Robust Threshold Logic Circuits – FRP	Spyros Tragoudas, Haibo Wang, Sarma Vrudhula	SIU/ ASU
2.5:	S7.Y5.XZ	Reliable Wireless Communications in Aircrafts and Other Challenging Environments	Xiangwei Zhou	SIU

Group 3

3.1:	A5.Y5.SV	Performance Optimal Control of a System of Interconnected Components Under Thermal and Energy Constraints	Sarma Vrudhula	ASU
3.2:	S2.Y5.LG	Registration and Fusion of EVS and SVS Runway Images for Embedded Systems	Lalit Gupta	SIU
3.3:	A3.Y5.YHL	Concurrency and Scheduling Analysis of Real-time Embedded Software on Multi-core Processors	Yann-Hang Lee	ASU
3.4:	S6.Y5.HW.ST	Adaptive Compressive Sensing Techniques for Low Power Sensors	Haibo Wang, Spyros Tragoudas	SIU
3.5:	A4.Y5.AS	Improving Usability of Multi-core DSPs	Aviral Shrivastava	ASU
N/A	A6.Y5.SV.SPIN	Spintronic Threshold Logic Array	Sarma Vrudhula	ASU