Center for Embedded Systems
An NSF Industry/University Cooperative Research Center

Synthesis and Design of Robust Threshold Logic Circuits

NSF Fundamental Research Project

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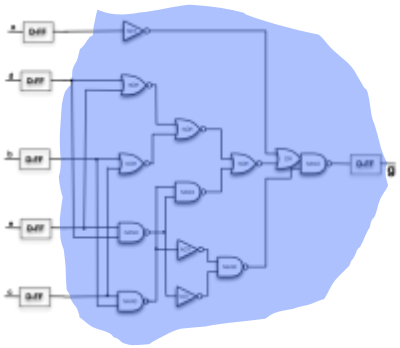
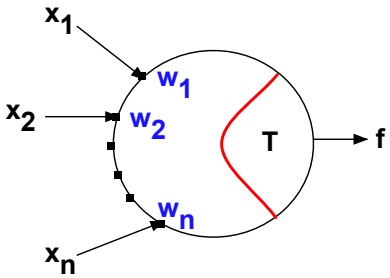
Project Overview and Description

- Threshold Functions

$$y = \begin{cases} 1 & \text{if } \sum_{i=1}^{n} w_i x_i \geq T \\ 0 & \text{otherwise} \end{cases}$$

- Threshold Gate: primitive cell that implements a threshold function





- Lower power, Lower Area Same or better Speed

- Major Challenges with TLGs
  - Sensitivity to Process Variations
  - Sensitivity to Mismatch
  - Low Voltage Operation
- ASU Focus:
  - Seamlessly integrate TLGs into mainstream digital design
- SIU Focus:
  - TLG Test Methodology
  - CMOS compatible TLG

Current Approach At SIUC

- **A new fault model for TLGs**
  - Enhanced Transition Fault Model to ensure maximum delay at the TL gate
  - An ATPG to detect defects at the TL circuit

- **Benefits to industry**
  - CMTL gates are easily manufactured and it is vital to identify delay defects efficiently

Current Approach At ASU

- **TLG Standard Cell Library**
  - Novel differential mode TLG architecture operating at 0.6V in 65nm
  - Development of non-volatile, Field Programmable Threshold Logic Array
- **Benefits to industry**
  - Seamless integration of TLGs with CMOS using existing commercial design flow

Project Tasks/ Deliverables

	Description	Date	Status
1	Min delay for MOBILE and CMTL gate designs	YR 1	Completed
2	Min gate and min delay for CMTL circuit synthesis	YR 1	Completed
3	Testability considerations in CMTL circuits	YR 2	In Progress
4	Design of FP Spintronic Threshold Logic Array	YR 1	Completed
5	Design of TLG with RROM for Low Voltage	YR 2	Completed
6	Simulations of TLG with RROM at 0.6V	YR 2	In Progress
7	Prototype TLG + RROM Fabrication	YR 2	Planned