Center for Embedded Systems
An NSF Industry/University Cooperative Research Center

Synthesis and Design of Robust Threshold Logic Circuits

Developments at SIUC

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Project Overview and Description

- **Work in Year 1**
  - Mobile or Current Mode Threshold Logic (CMTL) gate designs with minimum delay
  - Threshold Logic (TL) circuits with minimum number of TL gates and minimum circuit delay
- **Current focus:**

  Testability considerations in Current Mode Threshold Logic circuit implementations

Current approach

- **Novelty: A new fault model**
  - Enhanced Transition Fault Model to ensure maximum delay at the TL gate
  - An ATPG to detect defects at the TL circuit

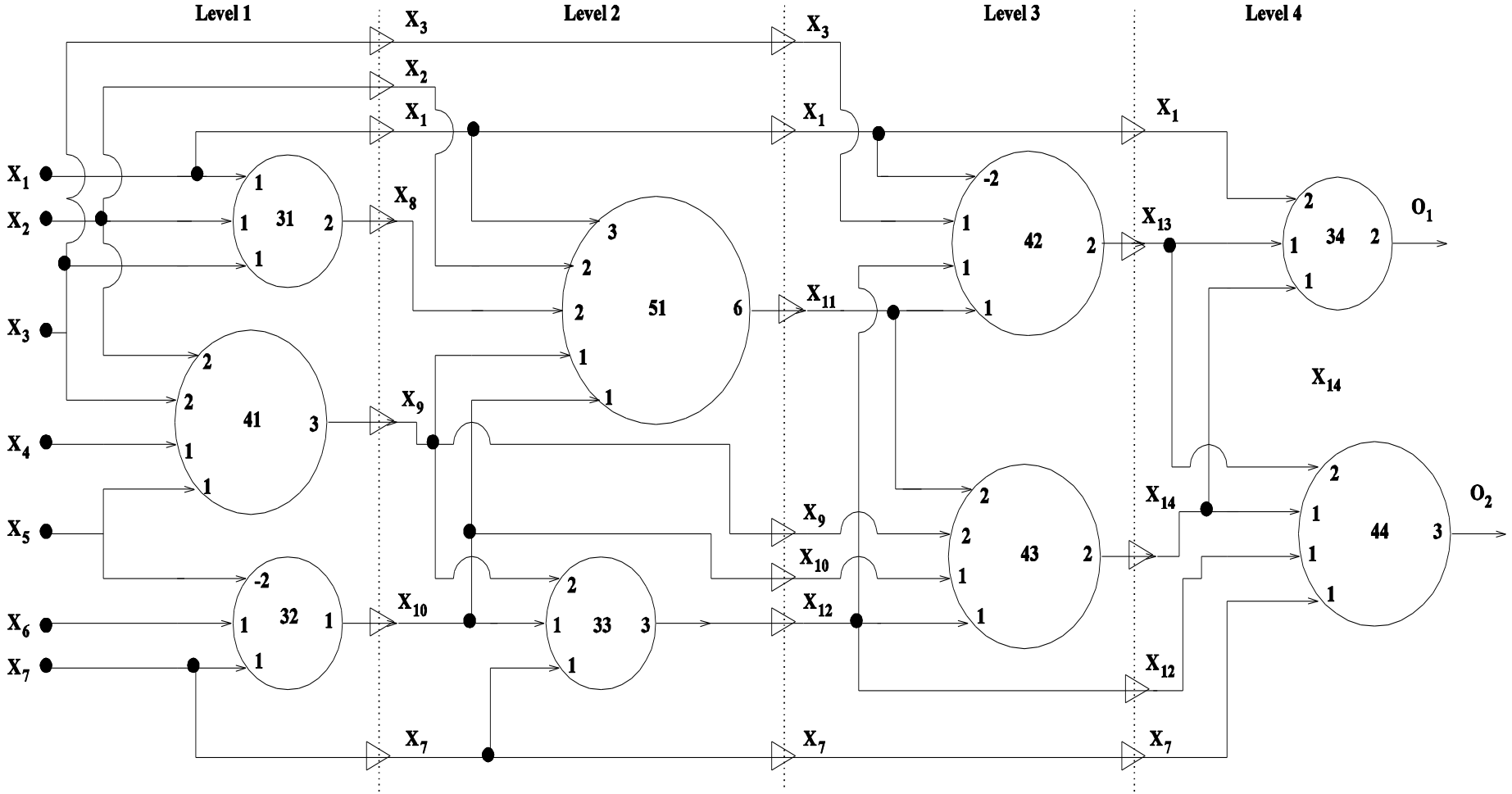
- **Benefits to industry:**
  - CMTL gates are easily manufactured and it is vital to efficiently identify delay defects

Project Status in Year 2

- Max Delay Transition Fault (MDTF) Model
  - Pattern sensitive model so that max delay is excited for each sensitized TF

- Developed an ATPG for the MDTF model for CMTL circuits

Project Status in Year 2

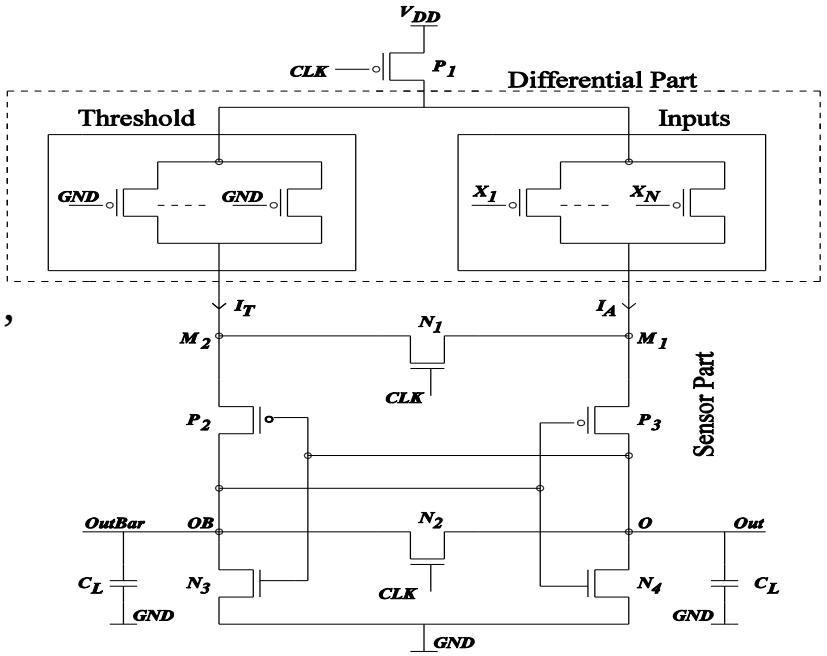


- At each pipeline level we select critical gate
  - **Example:** Gate 51 for 2nd stage
- ATPG is driven by the MDTF and an analytical model for the TL gate delay

Technical Detail on CML gates (Year 1)

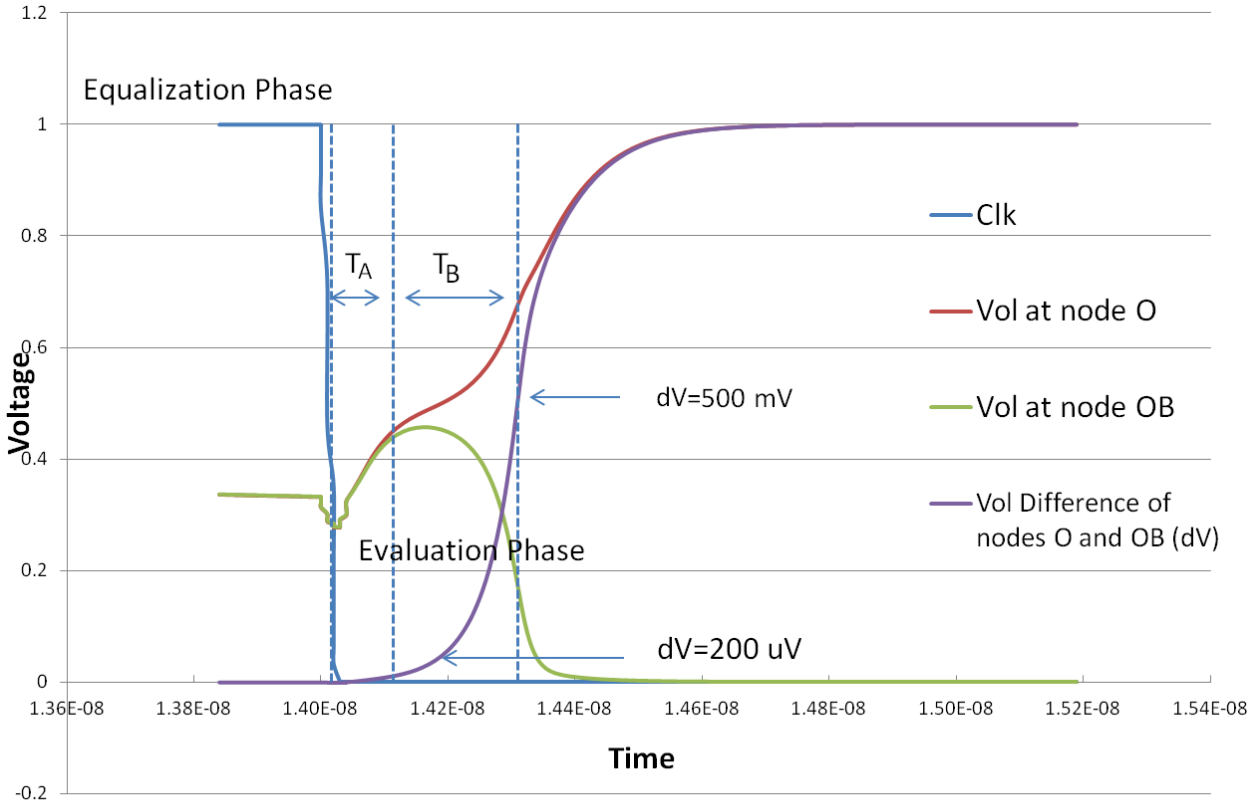
- **Current Mode Threshold Logic (CMTL) Gate**

  - Divided in to Differential part and Sensor part
  - Differential part consists of network of threshold transistors and input transistors
  - Total current from threshold part is I_T
  - Total current from input part (active transistors) is I_A
  - $I_A > I_T$, then Vout is logic High; $I_A < I_T$, then Vout is logic Low
  - CLK is applied clock



Technical Detail on CML gates (Year 1)

- **Operation of CMTL gate**
  - Operation of CMTL gate clock based
  - Clock is divided into two phases, equalization phase and evaluation phase
  - Delay of CMTL gate is the sum of activation time T_A and boosting time T_B



Technical Detail on CML gates (Year 1)

- For a given input configuration, where T, N, and S are given
- Assume current flowing through an active minimum sized PMOS is I_P
- Current flowing through threshold side of CMTLG is $I_T = T \cdot I_P$
- Current flowing through Input side of CMTLG for N_A (active inputs) is $I_A = N_A \cdot I_P$
- Hence, worst case delay for
  - Logic 1: $(I_A - I_T)$ should be minimum
  - Logic 0: $(I_T - I_A)$ should be minimum

Technical Detail on CM L gates (Year 1)

- **The obtained equation for delay of CMTLG is approximated by**

$$T_D = C_0 + C_1 \cdot S + C_2 \cdot \frac{1}{S} + \varepsilon$$

  - $C_0 = \frac{N}{N_A}(C_i' + C_T' + C_S') + \varepsilon_0$
  - $C_1 = C_S' \cdot \left|\frac{1}{N_A} - \frac{1}{T}\right| + \varepsilon_1$
  - $C_2 = N \cdot C_i' + T \cdot C_T' + \varepsilon_2$

  - C_i', C_T', C_S' are the unit capacitances of input weights, threshold weight, sensor
  - N, N_A, T are the Number of inputs, number of active inputs, threshold value

- **The obtained optimum sensor size by applying first derivative to T_D and equating it to zero is**

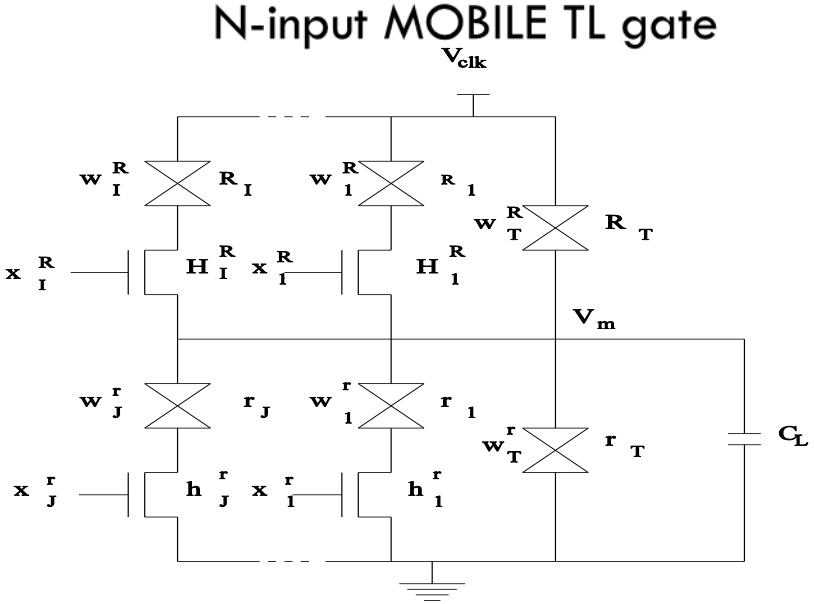
$$S_{opt} = \sqrt{\left(\frac{N \cdot C_i' + T \cdot C_T'}{C_S' \cdot \left|\frac{1}{N_A} - \frac{1}{T}\right|}\right)}$$

Technical Detail on MOBILE gates (Year 1)

- **Proposed an analytical model to approximate the transition time of a MOBILE TL gate**
- **The metric M is derived to approximate the transition time for an N-input MOBILE TL gate**
- $$M = \frac{k_r \cdot (w_T^R - w_T^r + \sum_{i=1}^{I}(w_i^R) - \sum_{j=1}^{J}(w_j^r)) + \sum_{i=1}^{I}(k_0 \cdot \omega_H + k_1 \cdot \omega_H \cdot w_i^R \cdot x_i^R) + C_L}{k_r \cdot (w_T^R + w_T^r + \sum_{i=1}^{I}(w_i^R \cdot x_i^R) + \sum_{j=1}^{J}(w_j^r \cdot x_j^r))}$$
- **The metric M can be used effectively to allocate weights that do not violate the functionality of TL gate and minimize the delay**
- **Minimizing the TL gate delay is done in three steps**
  - Step 1: Obtain inequalities which satisfy the functionality of the given TL gate
  - Step 2: Obtain inequalities for each pattern so that the metric M is less than a user defined value
  - Step 3: Plug the above inequalities in ILP solver to obtain the weights for given TL gate with min delay

Technical Detail on MOBILE gates (Year 1)

- **TL circuit implementation using MOBILE element**



- **The positive and negative threshold RTDs are denoted by R_T and r_T**
- **The positive and negative input weights are denoted by $W^{R}{}_{I}$ and $W^{r}{}_{J}$**
- **The positive and negative input pattern are denoted by $x^{R}{}_{I}$ and $x^{r}{}_{J}$**

Technical Detail on TL circuit synthesis (Year 1)

TLG Synthesis is currently bounded to a small number of inputs

- **ILP based methods [Jha 05]**
  - **Limited by ILP**
- **Decomposition based methods [Vrudhula 08 & Vrudhula 10]**
  - **Requires input function in complete sum form**
  - **Requires a specific variable ordering for each node function**
  - **These tasks are either space or time consuming and the explicit algorithms are not scalable.**

Technical Detail on TL circuit synthesis (Year 1)

- **Complete Sum (CS) : Sum of Prime Implicants.**
- **Variable Ordering (VO)**
  - f_k **: All prime implicants with exactly** k **number of literals**
  - f_k^{xi} **: Number of occurrences of an input variable** x_i **in** f_k
  - ***VO is*** $x_i \approx x_j$ **, when** $f_k^{xi} = f_k^{xj} \; \forall \; f_k$
  - ***VO is*** $x_i > x_j$ **, when** $f_k^{xi} > f_k^{xj}$ **in** f_k **with *smallest value of k***
- **Binary decision Diagram (BDD)**

  A function represented in a BDD is a DAG where the Shannon decomposition is carried out at each node. It does not contain vertices with either isomorphic sub-graphs or with both outgoing edges pointing to same node. A ZBDD is a version of BDD in which the node is removed if its positive edge is directed to the False node

Technical Detail on TL circuit synthesis (Year 1)

- **The contribution of the new method is an implicit scalable implementation of [Vrudhula 08], [Vrudhula 10] that requires appropriate algorithms and DS.**
- ***CS* and *VO* are done implicitly.**
- **Several other algorithms are designed implicitly.**
- **The proposed implicit methods uses BDD or ZBDD.**
- **The Synthesis Cost (TLG count) is decreased up to *40%* and on average around *20%* when working on larger functions instead of using small functions to build large functions (as existing methods do).**
- **The circuit delay is decreased up to *10%* and on average around *7%* .**
- **The proposed implicit methods are time efficient.**
- **Handle up to functions of up to 50 input variables, where as existing methods can only handle up to 8 input functions.**

Technical Detail on TL circuit synthesis (Year 1)

- There is an increased need to test for manufacturing defects and in particular, for delay defects in TL Circuits
- Each input pattern results in different rising or falling delay value for CMTL gate
- The input patterns are grouped based on the delay values and are calculated using the equation shown previously
- The proposed ATPG method generates a pair of vectors which ensures :
  - Maximum transition delay at the selected gate using MDFT model
  - Propagates the error latched caused by the delay defect to an observable point

References

- [Jha 05]: R. Zhang, P. Gupta, L. Zhong, and N. K. Jha, " Threshold network synthesis and optimization and its application to nanotechnologies ," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 24, no. 1, pp. 107–118, Jan 2005.*
- [Vrudhula 08]: T. Gowda and S. Vrudhula, " Decomposition based approach for synthesis of multi-level threshold logic circuits ," *In Proc. Asia and South Pacific Design Automation Conference, pp. 125-130, Mar 2008.*
- [Vrudhula 10]: T. Gowda, S. Vrudhula, N. Kulkarni, and K. Berezowski, " Identification of threshold functions and synthesis of threshold networks ," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 30, no. 5, pp.665-677, May 2011.*
- C.B. Dara, T. Haniotakis, S. Tragoudas, "Delay Analysis for an N-Input Current Mode Threshold Logic Gate," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2012, pp.344,349, 19-21 Aug. 2012.*
- C. B. Dara, S. Tragoudas, T. Haniotakis, "A Metric for Weight Assignment to Optimize the Performance of MOBILE Threshold Logic Gate," *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), pp.131-138, 3-5 Oct. 2011.*