I/UCRC Executive Summary - Project Synopsis	Date: 1/19/2012

Center: NSF I/UCRC for Embedded Systems

Project Title: Synthesis and Design of Robust Threshold Logic Circuits

Project Head (PI): Spyros Tragoudas	**Phone :** (618) 453 - 7027	**E-mail :**spyros@engr.siu.edu

Total NSF Request: $200,000	**Industry Investment:** $50,000

Project Description:

This project intends to address the fundamental challenges encountered in threshold logic (TL) circuits which have excellent potentials to outperform conventional CMOS circuits in terms of power dissipation and performance for future low-voltage low-power ASICs. This project takes a unified approach to simultaneously address TL circuit synthesis and TL gate design challenges, including process variation and noise. The proposed work will extended the application of TL circuits to Analog to digital converters (ADCs), an area that benefits from TL circuits have not been explored.

Experimental plan:

Circuit synthesis techniques and analytical models to assist the implementation of the gates of TL circuits as well as techniques that enable post-fabrication correction for CMOS TL circuits will be investigated. Previously developed synthesis techniques for robust TL circuits will be extended to systematically address the challenge of robust TL circuit design during logic synthesis, weight assignment and gate implementation. ADC circuits with using comparators with TL circuits will be developed.

Related work elsewhere:

Conventional TL circuits have been implemented and TL gate designs that use nontraditional nanoscale devices have been proposed. Recently, algorithms have been developed to optimally translate conventional Boolean functions into TL functions. In addition, synthesis algorithms have been developed for weight assignment to achieve robust TL circuit operations.

How this project is different:

The proposal addresses existing limitations on TL gate design and circuit synthesis techniques. Significant improvements in performance and power dissipation are anticipated as an outcome of the proposed activities. The vulnerability of TL circuits to process variation and circuit noise has not been addressed systematically and it will be examined during TL circuit synthesis as well as for the TL gate designs. Post-fabrication correction features in TL circuit designs and TL-based ADCs will be developed. Transition from traditional transistor-based implementations to styles that rely on future nanoscale devices, such as monostable-bistable logic elements, will be investigated.

Milestones:

1. **Milestone 1:** Analytical models to assist high performance and lower power TL gate designs for traditional and future nanoscale technologies by 7/31/2013
2. **Milestone 2:** Systematic synthesis approaches to optimally achieve robust TL circuits that incorporate post-fabrication correction features by 7/31/2014
3. **Milestone 3:** Development and demonstration of new ADC circuits with using TL circuits by 7/31/2014.

Deliverables:

1. Novel TL gate designs with post-fabrication correction features
2. Novel robust TL circuit synthesis approaches with improved performance and power dissipation characteristics
3. Novel ADC design with using TL circuits

How the project may be transformative and/or benefit society:

The developed circuit synthesis and gate design techniques will potentially impact drastically the implementation of ASICs using future nano-MOS technologies and beyond.

Research areas of expertise needed for project success:

1) logic synthesis; 2) digital design; 3) mixed-sign circuit; 4) device and process variations.

Potential Member Company Benefits:

The developed techniques can be easily adopted by the member companies.

Estimated Start Date: 8/1/2012	**Estimated Completion Date**: 7/31/2014

The Executive Summary is used by corporate stakeholders in evaluating the value of their leveraged investment in the center and its projects. It also enables stakeholders to discuss and decide on the projects that provide value to their respective organizations. **Ideally, the tool is completed and shared in advance of IAB meetings to help enable rational decision making.**