Center for Embedded Systems
An NSF Industry/University Cooperative Research Center

Center for Embedded Systems (CES)
Request for Proposals Template – YEAR 5

DUE: Monday, April 8, 2013, by 5 p.m.

TITLE:	**Multi-Partitioned Single Cores and Predictable Execution of Safety-Critical Tasks.**				
PI:	Dimitri Kagaris Harini Ramaprasad	**EMAIL:**	kagaris@engr.siu.edu harinir@siu.edu	**TEL:**	618-453-7973 618-453-4755
DEPT:	Electrical and Computer Engineering	**SCHOOL:**	Southern Illinois University Carbondale		

ABSTRACT: (250 OR FEWER WORDS)

The benefits offered by the consolidation of functionality in real-time embedded systems are currently counteracted by the need to preserve the criticality requirements of different tasks as they are sharing the same powerful processor ("core") or platform. These tasks may also be running in different operating systems ("partitions") under coordination from a hypervisor. The goal of this project is to investigate and characterize the level of interference between Highly Safety-Sensitive (HSS) and Less Safety-Sensitive (LSS) tasks running under the same or different operating systems on a single computational core, and accordingly develop scheduling algorithms to maintain the HSS requirements while providing acceptable Quality of Service to the LSS tasks.

PROBLEM:

The interference that HSS tasks experience in the presence of LSS tasks and other HSS tasks is challenging. The goal of this project is to investigate and characterize the level of interference between HSS and LSS tasks running under the same or different operating systems ("partitions") on a single computational core, and accordingly develop scheduling algorithms to maintain the HSS requirements while providing acceptable Quality of Service to the LSS tasks.

RATIONALE:

The results of the proposed study will be instrumental in enabling safe deployment of mixed-criticality tasks on multi-partitioned cores with hypervisor support.

APPROACH:

The PIs propose to employ a two-stage approach to ensure successful completion of this project:

1. In the first stage, the PIs propose to explore the interference between determinism and responsiveness of individual HSS and LSS tasks executing within the same operating system with specific emphasis on appropriate scheduling algorithms for ensuring the determinism of HSS tasks and the Quality-of-Service (QoS) for the LSS tasks.
2. In the second stage, the PIs propose to explore the interference between tasks running in a real-time operating system (RTOS) and a general-purpose operating system (GPOS) which are both running on a single core with hypervisor support and study the determinism and responsiveness of the operating systems in each case. In this stage of the project, the PIs propose to abstract details of task scheduling within each operating system and focus solely on scheduling across operating systems through the virtualization layer.

NOVELTY:

While multi-partitioned processors have been deployed in practice, they currently do not support dynamic scheduling and resource management. This project seeks to study the effects of such dynamic strategies.

POTENTIAL BENEFITS TO INDUSTRY MEMBERS:

Current practice in industry for safety-critical applications executing in a multi-partitioned processors rely entirely on a-priori scheduling of multiple partitions and tasks therein. The results of the proposed project will serve as a first step towards enabling dynamic task scheduling and resource management in multi-partitioned processors.

DELIVERABLES:

The deliverables for this project are as follows:

1. A comprehensive report detailing the qualitative and quantitative evaluation of different scheduling algorithms in terms of the achievable determinism and performance of the HSS and LSS tasks.
2. A comprehensive report detailing the interference of GPOS and RTOS on multi-partitioned cores with hypervisor support.
3. Modified hypervisor and operating system source code, if any.

TIMELINE/MILESTONES: (PER QUARTER)

The timeline for the first four quarters of this project is as follows:

1. Quarter 1: Exploration of existing research in the area of mixed-criticality systems and development/evaluation of new scheduling algorithms.
2. Quarter 2 &3: Characterization of HSS and LSS tasks executing in multiple partitions on a single core with hypervisor support (XEN, KVM).
3. Quarter 4: Report writing and technology transfer.

TECHNOLOGY TRANSFER:

Technology transfer will be performed in the form of comprehensive reports and updated hypervisor and operating system software.

BUDGET:

Funds in the amount of $25,000 are requested for:

1. Yearlong support for one graduate student
2. PI summer salaries
3. Travel to Industrial Advisory Board (IAB) meetings and member company locations for in-person meetings as required

BIBLIOGRAPHY: (ATTACH IN IEEE CONFERENCE OR JOURNAL FORMAT)

1. S. Xi, J. Wilson, C. Lu and C. Gill. “RT-XEN: Towards Real-Time Hypervisor Scheduling in Xen.” In Proceedings of the 9th ACM international conference on Embedded Software (EMSOFT), 2011.
2. Huber, B. ; El Salloum, C. ; Obermaisser, R. “A resource management framework for mixed-criticality embedded systems,’’ Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE.
3. C. Ault. “Challenges of safety-critical multi-core systems.” White paper, Wind River Research.
4. Hyun-Wook Jin ; Sanghyun Han, “Temporal partitioning for mixed-criticality systems”, Emerging Technologies & Factory Automation (ETFA), 2011 IEEE 16th Conference
5. Wasicek, A. ; El-Salloum, C. ; Kopetz, H., “A System-on-a-Chip Platform for Mixed-Criticality Applications,” Object/Component/Service-Oriented Real-Time Distributed Computing (ISORC), 2010 13th IEEE International Symposium
6. Jun Zhang; Kai Chen; Baojing Zuo; Ruhui Ma; Yaozu Dong; Haibing Guan, “Performance analysis towards a KVM-Based embedded real-time virtualization architecture.” 5th International Conference on Computer Sciences and Convergence Information Technology (ICCIT), 2010 , pp. 421 – 426.
7. Tamaş-Selicean, D. ; Pop, P., “Optimization of Time-Partitions for Mixed-Criticality Real-Time Distributed Embedded Systems,” Object/Component/Service-Oriented Real-Time Distributed Computing Workshops (ISORCW), 2011 14th IEEE International Symposium
8. Baruah, S. ; Bonifaci, V. ; D'Angelo, G. ; Li, H. ; Marchetti-Spaccamela, A. ; van der Ster, S. ; Stougie, L., “The Preemptive Uniprocessor Scheduling of Mixed-Criticality Implicit-Deadline Sporadic Task Systems,” Real-Time Systems (ECRTS), 2012 24th Euromicro Conference
9. Baruah, S. ; Fohler, G, “Certification-Cognizant Time-Triggered Scheduling of Mixed-Criticality Systems,” Real-Time Systems Symposium (RTSS), 2011 IEEE 32nd
10. Lemerre, M. ; Ohayon, E. ; Chabrol, D. ; Jan, M. ; Jacques, M.-B., “Method and Tools for Mixed-Criticality Real-Time Applications within PharOS,” Object/Component/Service-Oriented Real-Time Distributed Computing Workshops (ISORCW), 2011 14th IEEE International Symposium
11. Pathan, R.M., “Schedulability Analysis of Mixed-Criticality Systems on Multiprocessors,” Real-Time Systems (ECRTS), 2012 24th Euromicro Conference.
12. de Niz, D. ; Lakshmanan, K. ; Rajkumar, R., “On the Scheduling of Mixed-Criticality Real-Time Task Sets,” Real-Time Systems Symposium, 2009, RTSS 2009. 30th IEEE
13. Adventium Labs. “MiCART – Mixed-Criticality, Real-Time Virtualization Support.” www.adventiumlabs.com/?q=productsandservices/micart.

14. “Lmbench – Tools for Performance Analysis.” http://www.bitmover.com/lmbench/.
15. “MRTC WCET Benchmarks.” www.mrtc.mdh.se/projects/wcet/benchmarks.html.

PI INFORMATION: (ATTACH 2-PAGE CV)

Short Curriculum Vitae

DIMITRI KAGARIS

Professor

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Dimitri Kagaris received the Diploma degree in Computer Engineering and Informatics from the University of Patras, Greece, in 1988, and the M.S. and Ph.D. degrees in Computer Science from Dartmouth College, Hanover, New Hampshire, USA, in 1991 and 1994, respectively.

He is currently a full professor in the Electrical & Computer Engineering Department, Southern Illinois University, Carbondale, Illinois, USA. His research interests include design for testability of digital circuits, digital design automation, VLSI synthesis, and computer networks.

He has over 80 publications in peer-reviewed journals and conferences and has contributed chapters in scientific encyclopedias. He has been active in the area of Built-in Self-Test and Design for Testability since 1992. Part of his research has been supported by National Science Foundation (NSF). He has received twice the Outstanding Paper Award from the IEEE International Conference on Computer Design. He has served as a reviewer in major journals and conferences and has participated three times in NSF panels for the review and funding of Design Automation proposals.

List of 10 JOURNAL PUBLICATIONS

1. D. Nikolos, D. Kagaris, S. Sudireddy, S. Gidaros, ``An Improved Search Method for Accumulator-Based Test Set Embedding,'' **IEEE Transactions on Computers**, v. 58, n. 1, pp. 132 - 138, Jan. 2009.

2. J. Kakade, D. Kagaris, D.K. Pradhan, ``Evaluation of Generalized LFSRs as Test Pattern Generators in Two-Dimensional Scan Designs,'' **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, v. 27, n. 9, pp. 1689 - 1692, Sept. 2008.

3. J. Kakade, D. Kagaris, “Minimization of Linear Dependencies through the Use of Phase Shifters,” **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,** v. 26, n. 10, pp. 1877-1882, Oct. 2007.

4. D. Kagaris, P. Karpodinis, D. Nikolos, ``A Method for Accumulator-Based Test-per-Scan BIST," **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, v. 25, n. 11, pp. 2578-2586, Nov. 2006

5. D. Kagaris, S. Tragoudas, S. Kuriakose, “InTeRail: A Test Architecture for Core-Based SOCs,” **IEEE Transactions on Computers**, v. 55, n. 2, pp. 137-149, Feb. 2006.

6. D. Kagaris, “Phase Shifter Merging,” **Journal of Electronic Testing: Theory and Applications**, vol. 21, n. 2, pp. 161-168, April 2005.

7. D. Kagaris, “A Unified Method for Phase Shifter Computation**,” ACM Transactions on Design Automation of Electronic Systems**, vol. 10, no. 1, pp. 157-167, Jan. 2005.

8. D. Kagaris, “Multiple-Seed TPG Structures,” **IEEE Transactions on Computers**, vol. 52, no. 12, pp. 1633-1639, Dec. 2003.

9. D. Kagaris, S. Tragoudas “On the Non-Enumerative Path Delay Fault Simulation Problem,” **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, vol. 21, n. 9, pp. 1095-1100, Sep. 2002.

10. D. Kagaris, “Linear Dependencies in Extended LFSMs,” **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, vol. 21, n. 7, pp. 852-858, July 2002.

Harini Ramaprasad

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Professional Preparation

B.S.	Computer Science, Bangalore University, Bangalore, India, 2001
M.S.	Computer Science, North Carolina State University, Raleigh, North Carolina, 2006
Ph.D.	Computer Science, North Caroline State University, Raleigh, North Carolina, 2008

Research Interests

Real-time/Embedded Systems, Cyber-Physical Systems Operating Systems, Computer Architecture, Compilers

Appointments

Aug 2008 - present	Assistant Professor, Dept. of Electrical and Computer Engineering, Southern Illinois University Carbondale, Carbondale, Illinois
2002 - 2008	Research Assistant, North Carolina State University, Raleigh, North Carolina

Honors and Awards

Outstanding Teacher in the Department of Electrical and Computer Engineering for the year 2011.

Related and Significant Products

A. Choudhari, H. Ramaprasad, T. Paul, J. Kimball, M. Zawodniok, B. McMillin and S. Chellappan. "Stability of a Cyber-Physical Smart Grid Systems using Cooperating Invariants." To appear as a *full paper* in Proc. of the International Computer Software and Applications Conference (**COMPSAC**), 2013.

A. Sarkar, F. Mueller, H. Ramaprasad. "Static Task Partitioning for Locked Caches in Multi-Core Real-Time Systems." To appear in Proc. of the Conference on Compilers, Architecture and Synthesis for Embedded Systems (**CASES**), 2012.

O. Acevedo, D. Kagaris, K. Poluri, H. Ramaprasad and S. Warner. "Towards Optimal Design of Avionics Networking Infrastructures." In Proc. of the 31st Digital Avionics Systems Conference (**DASC**), 2012.

M. Shekhar, A. Sarkar, H. Ramaprasad and F. Mueller. "Semi-Partitioned Hard-Real-Time Scheduling Under Locked Cache Migration in Multicore Systems." In Proc. of the Euromicro Conference on Real-Time Systems (**ECRTS**), 2012.

A. Sarkar, F. Mueller and H. Ramaprasad. "Predictable Task Migration for Locked Caches in Multi-Core Systems". In Proc. of the ACM SIGPLAN Conference on Languages, Compilers and Tools for Embedded Systems (**LCTES**), 2011.

H. Ramaprasad and F. Mueller. "Tightening the Bounds on Feasible Preemptions". In Transactions on Embedded Computing Systems (**TECS**), Volume 10, Number 2, Article 27, December 2010.

A. Sarkar, F. Mueller, H. Ramaprasad and S. Mohan. "Push-Assisted Migration of Real-Time Tasks in Multi-Core Processors". In Proc. of the ACM SIGPLAN Conference of Languages, Compilers and Tools for Embedded Systems (**LCTES**), June 2009.

Synergistic Activities

Grant Review Panel Member

- National Science Foundation (NSF) – 2009, 2010, 2011, 2012

Program Chair
- Workshop on Energy-Aware Design and Analysis of Cyber-Physical Systems (**WEA-CPS**) – 2010

Track co-chair
- International Symposium on Electronic System Design (**ISED**) – 2011

Technical Program Committee member
- International Conference on Embedded Software (**EMSOFT**) – 2011
- Euromicro Conference on Real-Time Systems (**ECRTS**) – 2010, 2011, 2012, 2013
- Real-Time Systems Symposium (**RTSS**) – 2009, 2010, 2011, 2013
- International Conference on Embedded Computing (**EmbeddedCom**) – 2009
- Workshop on Cyber-Physical Systems (**WCPS**) – 2009
- International Conference on Embedded Software and Systems (**ICESS**) – 2009
- Real-Time and Embedded Technology and Applications Symposium (**RTAS**) – 2009, 2011
- International Symposium on Object and component-oriented Real-time distributed Computing (**ISORC**) – 2012, 2013
- International Conference on Embedded and Real-Time Computing Systems and Applications (**RTCSA**) – 2013
- International Conference on Real-Time Networks and Systems (**RTNS**) – 2013

External reviewer
- Real-Time and Embedded Technology and Applications Symposium (**RTAS**) – 2010
- Euromicro Conference on Real-Time Systems (**ECRTS**) – 2003, 2004, 2006, 2008, 2009
- IEEE Real-Time Systems Symposium (**RTSS**) – 2006, 2008
- Workshop on Worst-Case Execution Time Analysis (**WCET**) – 2006
- ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems (**LCTES**) – 2006, 2007, 2008
- IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (**RTCSA**) – 2006
- International Conference on Parallel and Distributed Systems (**ICPADS**) - 2006
- International Parallel and Distributed Processing Symposium (**IPDPS**) – 2009
- International Conference on Compilers, Architecture and Synthesis for Embedded Systems (**CASES**) – 2008, 2009
- ACM Transactions on Embedded Computing Systems (**TECS**)
- IEEE Transactions on Computers (**TC**)
- IEEE Transactions on Parallel and Distributed Systems (**TPDS**)
- ACM Transactions on Architecture and Code Optimization (**TACO**)
- Design Automation for Embedded Systems (**DAEM**)

Research Collaborators
- Frank Mueller (North Carolina State University)
- Yuan Xie (Penn State University)
- Aviral Shrivastava (Arizona State University)
- Jonathan Kimball, Maciej Jan Zawodniok, Bruce McMillin, Sriram Chellappan (Missouri University of Science and Technology)
- Spyros Tragoudas, Dimitrios Kagaris, Ning Weng, Haibo Wang (Southern Illinois University Carbondale)
- Wei Zhang (Virginia Commonwealth University)

Graduate Advisor
- Frank Mueller (North Carolina State University)

Thesis Advisor
- MS, Southern Illinois University Carbondale:
  (Completed) Kedar Katre, Vardhman Jain Pukhraj Jain, Aravind Mysore Chandrashekar, Robin Rajkumar
  (Current) Kaushik Poluri
- PhD, Southern Illinois University Carbondale:
  (Current) Mayank Shekhar, Sankalpanand Motakpalli, SatyaMohan Raju Gudidevuni, Ashish Choudhari, Aishwarya Vasu, Kiriti Nagesh Gowda

I/UCRC Executive Summary - Project Synopsis		Date:
Project Title: Multi-Partitioned Single Cores and Predictable Execution of Safety-Critical Tasks.		
Center/Site: Center for Embedded Systems/Southern Illinois University Carbondale		
Principle Investigator: Dimitri Kagaris Harini Ramaprasad		**Type: New**
Tracking No.: (CES office to input)	**Phone :** 618-453-7973 618-453-4755	**E-mail :** kagaris@engr.siu.edu harinir@siu.edu
		Proposed Budget: $25,000

Abstract: The benefits offered by the consolidation of functionality in real-time embedded systems are currently counteracted by the need to preserve the criticality requirements of different tasks as they are sharing the same powerful processor ("core") or platform. These tasks may also be running in different operating systems ("partitions") under coordination from a hypervisor. The goal of this project is to investigate and characterize the level of interference between Highly Safety-Sensitive (HSS) and Less Safety-Sensitive (LSS) tasks running under the same or different operating systems on a single computational core, and accordingly develop scheduling algorithms to maintain the HSS requirements while providing acceptable Quality of Service to the LSS tasks.

Problem: The interference that HSS tasks experience in the presence of LSS tasks and other HSS tasks is challenging. The goal of this project is to investigate and characterize the level of interference between HSS and LSS tasks running under the same or different operating systems ("partitions") on a single computational core, and accordingly develop scheduling algorithms to maintain the HSS requirements while providing acceptable Quality of Service to the LSS tasks.

Rationale / Approach: The PIs propose to employ a two-stage approach to ensure successful completion of this project. In the first stage, the PIs propose to explore the interference between determinism and responsiveness of individual HSS and LSS tasks executing within the same operating system with specific emphasis on appropriate scheduling algorithms for ensuring the determinism of HSS tasks and the Quality-of-Service (QoS) for the LSS tasks. In the second stage, the PIs propose to explore the interference between tasks running in a real-time operating system (RTOS) and a general-purpose operating system (GPOS) which are both running on a single core with hypervisor support and study the determinism and responsiveness of the operating systems in each case. In this stage of the project, the PIs propose to abstract details of task scheduling within each operating system and focus solely on scheduling across operating systems through the virtualization layer.

Novelty: While multi-partitioned processors have been deployed in practice, they currently do not support dynamic scheduling and resource management. This project seeks to study the effects of such dynamic strategies.

Potential Member Company Benefits: Current practice in industry for safety-critical applications executing in a multi-partitioned processors rely entirely on a-priori scheduling of multiple partitions and tasks therein. The results of the proposed project will serve as a first step towards enabling dynamic task scheduling and resource management in multi-partitioned processors.

Deliverables for the proposed year: The deliverables for this project are as follows: 1) A comprehensive report detailing the qualitative and quantitative evaluation of different scheduling algorithms in terms of the achievable determinism and performance of the HSS and LSS tasks. 2) A comprehensive report detailing the interference of GPOS and RTOS on multi-partitioned cores with hypervisor support. Modified hypervisor and operating system source code, if any.

Milestones for the proposed year: Q1: Exploration of existing research in the area of mixed-criticality systems and development/evaluation of new scheduling algorithms. Q2 & Q3: Characterization of HSS and LSS tasks executing in multiple partitions on a single core with hypervisor support (XEN, KVM). Q4: Report writing and technology transfer.

Progress to Date: THIS SECTION TO BE UPDATED IN JANUARY

Estimated Start Date: 08/15/2013	**Estimated Knowledge Transfer Date**: 08/31/2014