Center for Embedded Systems (CES)
Request for Proposals Template – YEAR 5

DUE: Monday, April 8, 2013, by 5 p.m.

TITLE:	Ground Work for Embedding a Field Oriented Motor Controller into a Single System on a Chip				
PI:	C.J. Hatziadoniu	**EMAIL:**	hatz@siu.edu	**TEL:**	(618) 453-7036
DEPT:	Electrical and Computer Engineering	**SCHOOL:**	Engineering		

ABSTRACT: (250 OR FEWER WORDS)

This project will develop a high performance SoC FPGA with embedded microprocessor and logic to implement a field oriented control (FOC) motor drive. The SoC includes a multi core micro-processor and an FPGA. The FPGA will incorporate the low level computationally intensive parts of the controller; the micro-processor will integrate the high level control functions and the supervisory functions. The proposed work will develop a suitable implementation of the FOC into the FPGA. The main problems addressed by this work include achieving high control band-width and closed-loop accuracy under the limited resources of the FPGA. The results of this investigation can be later extended to build and test a complete prototype system.

PROBLEM:

Motor drives often require fast-acting control loops in order to achieve fast, accurate and stable response. Particularly for FOC the computation requirements can be intense. Therefore, conventional implementations based on digital processors or micro-controllers may not always provide the control bandwidth necessary for the application. On the other hand, SoC FPGA systems with embedded processing offer the capability for fast computation and increased data acquisition rates. The project will investigate the design of a FOC loop into a SoC which combines a micro-processor and an FPGA.

RATIONALE:

The work performed by the project will provide results that can be used for building a complete motor control system.

APPROACH:

FOC can provide quick and fast adjustment of the motor torque and speed by precisely controlling the current components related to the field and torque of the motor [1-3]. Application of a FOC loop requires however intense computation involving compensation for the motor internal impedance, frame of reference transformations and a vector-based or PWM-based grid control for the inverter.

Conventional FOC implemented in digital micro-controllers has a limited band-width and therefore limited response time due to the limited resources and computational speed of the micro-controller. An FPGA implementation of FOC, on the other hand, can dramatically improve the control bandwidth [1, 2] allowing for faster response times.

This work will study the development of a FOC suitable for an FPGA system. The basic parts of the FOC for a motor drive include: (a) the data acquisition system, (b) the resolver-to-digital converter (RDC) and (c) the main computational blocks for the FOC algorithm [1,2]. Furthermore, the latter include the frame-of-reference transformations of the motor currents, the PI control blocks of the motor direct and quadrature current

components and an additional frame-of-reference transformation of the stator voltages to eventually derive the gate pulse for the inverter under a suitable PWM scheme.

The RDC has been already developed and successfully tested for a microcontroller application as part of a recent project sponsored by the Center. This work will migrate the developed RDC into the FPGA.

Even though many FPGA systems include a data acquisition component, operation in noisy environment and particularly ground noise can deteriorate the data conversion accuracy. The proposed work will consider external data acquisition in order to minimize input noise.

Specifically, the proposed work will develop a suitable mathematical model for design a stable FOC loop with the desired response characteristics. Subsequently, the designed loop will be transferred onto the FPGA [3]. The FPGA configuration will include a set of registers allocated for values such as gains, controller parameters and controller set points that will be furnished by the supervisory micro-processor, which is part of the SoC. In order to obtain the optimum outcome, studies will conducted to investigate the trade-off between the bit size of the number representation in the FPGA versus available resources inside the FPGA and versus the resulting control bandwidth reduction, noise sensitivity and parameter error sensitivity.

NOVELTY:

The novelty of the proposed project lies in the development of design methods for an FPGA-based FOC and in the combination of digital microcontroller and logic within an FPGA which is expected to provide improved flexibility for motor controller design.

POTENTIAL BENEFITS TO INDUSTRY MEMBERS:

The project will lay the groundwork for a subsequent development and testing of a complete motor drive controller including high-level functions. The project benefits electronics, heavy machinery, aerospace and other industries.

DELIVERABLES:

The following are the project deliverables:
(a) Integration of the RDC into the FPGA;
(b) An FPGA-based FOC algorithm.

TIMELINE/MILESTONES: (PER QUARTER)

The following are the milestones of the project:

Task	Quarter 1	Quarter 2	Quarter 3	Quarter 4
Integration of RDC				
FOC feasibility study				
FOC algorithm and testing				

TECHNOLOGY TRANSFER:

The results of the proposed project can be transfer directly to existing SoC modules of appropriate size.

BUDGET:

The budget requested for this project is $25k, for the PI and one half-time graduate student.

BIBLIOGRAPHY: (ATTACH IN IEEE CONFERENCE OR JOURNAL FORMAT)

[1] Lahoucine Idkhajine, Eric Monmasson, Mohamed Wissem Naouar, Antonio Prata, and Kamel Bouallaga, "Fully Integrated FPGA-Based Controller for Synchronous Motor Drive", IEEE Trans. On Industrial El., Vol. 56-10, Oct. 2010, pp 4006-17.

[2] Mohd. Marufuzzaman, M.B.I. Reaz, M.A. Mohd. Ali, FPGA implementation of an intelligent current dq PI controller for FOC PMSM drive", Proc. 2010 International Conf. on Computer Applications and Industrial Electronics (ICCAIE 2010), Dec. 5-7, 2010, Kuala Lumpur, Malaysia, pp 602-5.

[3] Amit Kumar Jain, and V. T. Ranganathan, "Modeling and Field Oriented Control of Salient Pole Wound Field Synchronous Machine in Stator Flux Coordinates", IEEE Trans. On Industrial El., Vol 58-3, March 2011, pp 960-70.

PI INFORMATION: (ATTACH 2-PAGE CV)

CONSTANTINE J. HATZIADONIU, Professor, hatz@siu.edu
Electrical and Computer Engineering at Southern Illinois University
1230 Lincoln Dr.
Carbondale, IL 62901-6603

Education

Diploma in Electrical Eng., University of Patras, Greece, 1983
Ph.D. in Electrical Eng., West Virginia University, Morgantown, 1987

Professional Experience

- Professor of Electrical and Computer Engineering, Southern Illinois University Carbondale. July 2003-present.
- Associate Professor in the Department of Electrical and Computer Engineering, Southern Illinois University Carbondale. August 1993-2003.
- Assistant Professor in the Department of Electrical Engineering, Southern Illinois University Carbondale. August 1989-August 1993.
- Visiting Assistant Professor in the Department of Electrical Engineering, Southern Illinois University Carbondale. September 1987-1989.
- Teaching and Research Assistant. Department of Electrical Engineering, West Virginia University, Morgantown. August 1984-1987.
- Consulting engineer, Greece. August 1983-1984.

Research Interests

Power electronics, Energy harvesting devices, wind and photovoltaic energy systems, power system modeling and simulation; power system control and protection.

Recent Publications.

C.J. Hatziadoniu, N.B. Harp, and A.J. Sugg, "Finite-Element Models for Open-Air Power Lines in Broadband PLC", IEEE Trans. On Power Delivery, Vol. 21, No. 4, Oct. 2006, pp. 1898-1904.

Hany A. Abdelsalam and **C.J. Hatziadoniu**, "A Robust Wide Area Controller of Multiple FACTS for Damping Oscillations in Multi-Area Power System Using the H∞ Method", Power System Conference 2011 PSC11, March 15-18, 2011 at Clemson University, Clemson, SC, USA.

F. Pourboghrat, F. Farid, C.J. **Hatziadoniu**, M. Daneshdoost, F. Mehdian, M. Lotfalien, "Local Sliding Control for Damping Inter-Area Power Oscillations", IEEE Trans. On Power Systems, PES 19-2, May 2004, pp. 1123-34.

A. Albanna and **C.J. Hatziadoniu**, 'Harmonic Modeling of Hysteresis Inverters in the Frequency Domain', IEEE Trans. on Power Electronics, Vol. 25, No 5, May 2010, pp.1110-4.

Ahmad Albanna, **C.J. Hatziadoniu**, "Harmonic Modeling and Analysis of Multiple Residential Photo-Voltaic Generators", Power and Energy Conference, University of Illinois Urbana-Champaign, February 2010.

Ahmed Albanna, **C.J. Hatziadoniu**, "Harmonic Modeling of Three-Phase Neutral-Point Inverters", Proceedings of the 2009 North American Power Symposium, Mississippi State University, Starkville, MS, Oct 4-6, 2009.

Ahmed Albanna, **C.J. Hatziadoniu**, "Harmonic Modeling of Single-phase Three-level Hysteresis Inverters", Proceedings of the 2009 North American Power Symposium, Mississippi State University, Starkville, MS, Oct 4-6, 2009.

G. Chang, **C.J. Hatziadoniu**, W. Xu, P. Ribeiro, R. Burch, W.M. Grady, M. Halpin, Y. Liu, S. Ranade, D. Ruthman, N. Watson, T. Ortmeyer, J. Wikston, A, Medina, A. Testa, R. Gardinier, V. Dinavahi, F. Acram, P. Lehn, "Modeling Devices with nonlinear Voltage-current Characteristics for harmonic studies", IEEE Trans. On Power Delivery, Vol. 19, No. 4, Oct. 2004, pp. 1802-11.

Synergetic Activities.

- "Pilot Study of Energy Harvesting Devices towards the Development of a Prototype", (PI C.J. Hatziadoniu, Co-PI Tsuchin Chu and Fran Harackiewicz), NSF, I/UCRC for Embedded Systems August 2012-August 2013.
- "Resolver Sensor Conditioning Size Reduction", (PI C.J. Hatziadoniu, Co-PI W. Haibo), NSF, I/UCRC for Embedded Systems, August 2012-August 2013.
- "Distribution System Modeling for Power Line Communication", Research grant, AMEREN-UE, 2001-2002.
- "Software for the optimum operation and planning of high-data rate PLC Systems", Research grant, AMEREN-UE 2003-04.
- "Workstation Computer Program for Insulation Coordination of ac and dc Substations"
- Research grant (EPRI 1989-1992), RP 2323, with G.D. Galanos and M. Daneshdoost.
- "Advanced Voltage Systems", Research grant (EPRI 1990-1992), RP 4000-22, with G.D. Galanos and F. Pourboghrat.
- "Faraday's Law Electric Machine Laboratory", Equipment grant (NSF 1991), with G.D. Galanos, V. Feiste and M Daneshdoost.

Collaborators and Other Affiliations.

Collaborators: D. Takach, Ameren UE, Saint Louis, Missouri.
Graduate Advisor: Dissertation Advisor: G.D. Galanos, Department of Electrical and Computer Engineering, SIUC.
Thesis and Dissertation Advisor (recent): A. Albana (PhD), H. Ahmed (PhD), Dler Dler (MS), H. El-Hadji (MS), D. Schleeper (MS).

I/UCRC Executive Summary - Project Synopsis	Date:

Project Title: Ground Work for Embedding a Field Oriented Motor Controller into a Single System on a Chip

Center/Site: I/UCR Center for Embedded Systems

Principle Investigator: C.J. Hatziadoniu	Type: New
Tracking No.: (CES office to input) **Phone :618-453-7036**	**E-mail :hatz@siu.edu**
	Proposed Budget: $25,000

Abstract: This project will develop a high performance SoC FPGA with embedded microprocessor and logic to implement a field oriented control (FOC) motor drive. The SoC includes a multi core micro-processor and an FPGA. The FPGA will incorporate the low level computationally intensive parts of the controller; the micro-processor will integrate the high level control functions and the supervisory functions. The proposed work will develop a suitable implementation of the FOC into the FPGA. The main problems addressed by this work include achieving high control band-width and closed-loop accuracy under the limited resources of the FPGA. The results of this investigation can be later extended to build and test a complete prototype system.

Problem: Motor drives often require fast-acting control loops in order to achieve fast, accurate and stable response. Particularly for FOC the computation requirements can be intense. Therefore, conventional implementations based on digital processors or micro-controllers may not always provide the control bandwidth necessary for the application. On the other hand, SoC FPGA systems with embedded processing offer the capability for fast computation and increased data acquisition rates. The project will investigate the design of a FOC loop into a SoC which combines a micro-processor and an FPGA.

Rationale / Approach: The work performed by the project will provide results that can be used for building a complete motor control system. The proposed work will develop a suitable mathematical model for design a stable FOC loop with the desired response characteristics. Subsequently, the designed loop will be transferred onto the FPGA. The FPGA configuration will include a set of registers allocated for values such as gains, controller parameters and controller set points that will be furnished by the supervisory micro-processor, which is part of the SoC. In order to obtain the optimum outcome, studies will conducted to investigate the trade-off between the bit size of the number representation in the FPGA versus available resources inside the FPGA and versus the resulting control bandwidth reduction, noise sensitivity and parameter error sensitivity.

Novelty: The novelty of the proposed project lies in the development of design methods for an FPGA-based FOC and in the combination of digital microcontroller and logic within an FPGA which is expected to provide improved flexibility for motor controller design.

Potential Member Company Benefits: The project will lay the groundwork for a subsequent development and testing of a complete motor drive controller including high-level functions. The project benefits electronics, heavy machinery, aerospace and other industries.

Deliverables for the proposed year:
The following are the project deliverables:
(a) Integration of the RDC into the FPGA;(b) An FPGA-based FOC algorithm.

Milestones for the proposed year:

Task	Quarter 1	Quarter 2	Quarter 3	Quarter 4
Integration of RDC				
FOC feasibility study				
FOC algorithm testing				

Progress to Date: THIS SECTION TO BE UPDATED IN JANUARY

Estimated Start Date: August 15, 2013	**Estimated Knowledge Transfer Date**: