Center for Embedded Systems (CES)
Request for Proposals Template – YEAR 5

DUE: Monday, April 8, 2013, by 5 p.m.

TITLE:	**Adaptive compressive sensing techniques for low power sensors**				
PI:	Haibo Wang and Spyros Tragoudas	**EMAIL:**	{haibo, Spyros}@engr.siu.edu	**TEL:**	618-453-1522 618-453-7645
DEPT:	ECE	**SCHOOL:**	Southern Illinois University		

ABSTRACT: (250 OR FEWER WORDS)

The objective of this project is to investigate novel adaptive approaches to more effectively apply compressive sensing techniques [1, 2] in low-power sensor systems. Recently, compressive sensing emerged as an attractive technique in low-power sensor development [3, 4, 5], because of its capability to allow sensor signals to be sampled at rates lowers than Nyquist rate. In compressive sensing, the number (denoted as M) of sampled compressive signals is selected according to the sparseness (to elaborated in the Problem section) of the sensor signals. Currently, the majority of compressive sensing circuits assume fixed M values during the entire sensing operations. To further reduce the power consumption of sensors using compressive sensing, we have been investigating the potentials of adaptively adjusting the sampling rates used in compressive sensing methods at system level. As a natural extension to the current effort, the proposed research is to investigate circuit techniques to execute adaptive compressive sensing at sensor nodes. Particularly, we will investigate the use of low-power analog wavelet transformation circuit to detect when sampling rate can be changed in adaptive compressive sensing.

PROBLEM:

The theory of compressive sensing is first briefly explained as follows. Assume vector X contains N sampled sensor outputs in time domain. The values of X are plotted in the top panel of Figure 1. Assume Ψ is *NXN* matrix that projects X into another domain with projected values contained in vector α. Hence we have:

$$X = \Psi \bullet \alpha$$

Note that α is also a vector with the size of N. However, if α contains only K significant terms and the rest of N-K terms are zero or insignificant as shown in the bottom panel of Figure 1, sensor signal X is called sparse or compressible (the sparseness refers to the value of K compared to N).

For compressible signal X, compressive sensing produces compressed output Y using the following matrix operation:

$$Y = \Phi \bullet X$$

where Y is a vector with the size of M and Φ is an M×N matrix. For sensor signal X, if its corresponding α projection has only K significant terms, and Ψ and Φ are incoherent, the value of M that enables the receiver to reconstruct X from Y is:

$$M = \mathrm{O}(K \log \frac{N}{K})$$

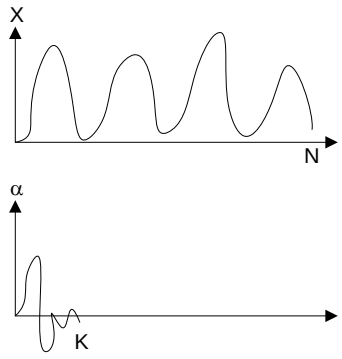

Figure 1: A compressible signal.

If K<<N, then M<N, which implies that the sensor outputs can be potentially sampled at rates less than Nyquist rates. Currently, most compressive sensing circuits are designed with fixed M values. If signal sparseness characteristic changes during sensor expected life cycle, this may result in different K values and hence it is desirable to use different M values.

For compressive sensing circuits designed with fixed M values, such variations potentially degrade the sensor performance in terms of either accuracy or power efficiency.

RATIONALE:

We have been investigating the sparsity variations for signals collected by biomedical sensors. Our study indicates that signal sparsity varies over the time and at different operating conditions. As an example, the signal sparisty variation for ECG (electrocardiogram) signal is shown in Figure 2. We are also working on estimating the potential power saving if the sampling rate used in compressive sensors can be adaptively adjusted according to signal sparsity variations, which also indicates that adaptive compressive sensing is an attractive technique for further reducing power consumption of sensor nodes. An import question that needs to be answered in the implementation of adaptive compressive sensing method is how to detect the signal sparsity variations and subsequently adjust the sampling rate. This motivates the proposed research.

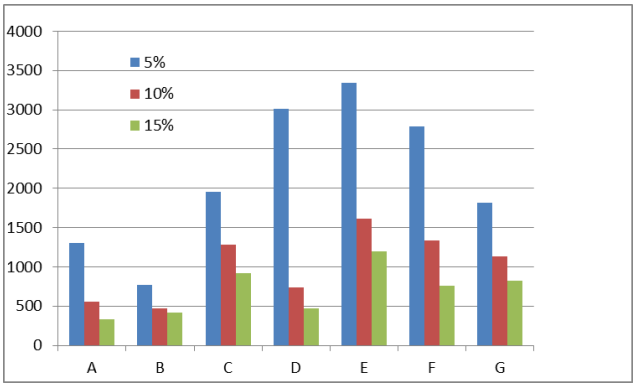

Figure 2 Signal sparsity variations

APPROACH:

To address the above challenge, we propose to use a low-power analog (continuous-time) wavelet transformation (WT) circuit to monitor the signal sparsity during sensor operation and to adjust the sampling rates according to the output of the analog WT circuit. To experimentally validate this approach, we will first develop an analog WT circuit, and then establish the relation between the analog WT circuit output and the signal sparsity. Based on the simulation results, we will develop a behavior model for the analog WT circuit, which models the circuit power consumption and its ability to detect signal sparsity for different types of signals. This model will be incorporated into the simulation framework that is currently being developed.

Recently, a number of analog WT circuits have been reported for signal processing applications [6, 7, 8]. Such circuits are typically optimized for high accuracy. Unlike theses designs, the analog WT circuit here is used to give indications about signal sparsity and hence we have more relaxed tolerances on circuit accuracy and throughput but prefer low power consumption. In the circuit development phase, research efforts will be directed toward investigating low-power circuit techniques for analog WT circuits. The circuit will be developed using a 0.13μm CMOS technology. Once the analog WT circuit is developed, extensive circuit simulations will be performed with EEG (Electroencephalography) and ECG signals as circuit input. Such signals are obtained from Multi-parameter Intelligent Monitoring in Intensive Care (MIMIC II) database (http://physionet.org) and will be converted into analog format for circuit simulation. We already studied the sparsity of these signals in our current study. Through circuit simulations, we aim to establish the relations between the analog WT circuit output and the sparsity of the signals. Finally, the findings obtained in circuit simulations will be encapsulated into a behavior model, which will be integrated into the adaptive compressive sensing simulation framework that is currently under development. Subsequently, system-level simulations will be performed to investigate the effectiveness of the proposed approach.

NOVELTY:

Compressive sensing is a relatively new approach to reduce the power consumption of certain type sensors. The proposed work helps make compressive sensing more power efficiency, hence advances the state of the art of compressive sensing.

POTENTIAL BENEFITS TO INDUSTRY MEMBERS:

The developed techniques have the potentials to help member companies further reduce the power consumptions of certain sensor devices in productions or used in their research and development (R&D) projects.

DELIVERABLES:

1. Design of the analog wavelet transformation circuit
2. Investigation results on the effectiveness of using analog wavelet transformation circuit to determine the sampling rates in adaptive compressive sensing

TIMELINE/MILESTONES: (PER QUARTER)

1. **Quarter 1 (08/13-10/13):** Finalize the structure and complete the key optimization issues for the circuit to be designed
2. **Quarter 2 (11/13-01/14):** Complete the circuit design
3. **Quarter 3 (02/13-04/13):** Establish the relation between circuit output and signal sparsity via extensive circuit simulations; and encapsulate the findings into a behavior models
4. **Quarter 4 (05/13-07/14):** Investigate the effectiveness of the proposed approach

TECHNOLOGY TRANSFER:

1. Low-power circuit techniques for implementing continuous-time wavelet transformation circuits
2. Knowledge on using continuous-time wavelet transformation circuit to monitor signal sparsity and subsequently determine optimal sampling rate for adaptive compressive sensing

BUDGET:

The requested budget is $50,000. Among them, $29,052 is to support PhD students (1 student @50% for 12 months, 1 student @25% for 12 months) and $20,948 is for the salaries of the two PIs and travel. ***SIUC match: $94,271*** ($22,750 on indirect cost waiver and $71,521.5 on PhD student tuition waiver).

BIBLIOGRAPHY: (ATTACH IN IEEE CONFERENCE OR JOURNAL FORMAT)

1. D. Donoho, “Compressed sensing,” IEEE Transactions on Biomedical Engineering, Vol. 52, No. 4, pp. 1289–1306, April 2006.
2. E. Candes, J. Romberg, and T. Tao, “Stable signal recovery from incomplete and inaccurate measurements,” Communications on Pure and Applied Mathematics, Vol. 59, No. 8, pp. 1207–1223, August 2006.
3. Allstot, E.G.; Chen, A.Y.; Dixon, A.M.R.; Gangopadhyay, D.; Allstot, D.J.; "Compressive sampling of ECG bio-signals: Quantization noise and sparsity considerations," 2010 IEEE Biomedical Circuits and Systems Conference (BioCAS), pp. 41-44, Nov. 2010.
4. Chen, F.; Chandrakasan, A.P.; Stojanovic, V.; "A Signal-agnostic Compressed Sensing Acquisition System for Wireless and Implantable Sensors," 2010 IEEE Custom Integrated Circuits Conference (CICC), pp. 1-4, Sept. 2010.
5. Baheti, P.K.; Garudadri, H.; "An ultra-low power pulse oximeter sensor based on compressed sensing," Sixth International Workshop on Wearable and Implantable Body Sensor Networks, pp. 144-148, 2009.
6. Edwards, R.T.; Godfrey, M.D., "An analog wavelet transform chip," Neural Networks, 1993., IEEE International Conference on , vol., no., pp.1247,1251 vol.3, 1993.
7. Sánchez-López, C.; Diaz-Sanchez, A.; Tlelo-Cuautle, E., "Analog implementation of MOS-translinear Morlet Wavelets," Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on , vol.1, no., pp.I-393,I-396 vol.1, 25-28 May 2003
8. Karel, J. M H; Haddad, S. A P; Hiseni, S.; Westra, R.L.; Serdijn, W.A.; Peeters, R. L M, "Implementing Wavelets in Continuous-Time Analog Circuits With Dynamic Range Optimization," Circuits and Systems I: Regular Papers, IEEE Transactions on , vol.59, no.2, pp.229,242, Feb. 2012.

PI INFORMATION: (ATTACH 2-PAGE CV)

Haibo Wang

Department of Electrical and Computer Engineering
Southern Illinois University, Carbondale, IL 62901-6603
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Professional Preparation:

University of Arizona, Tucson	Ph.D.	Electrical and Comp. Engineering	5/02
Nanyang Technological Univ., Singapore	M. Eng.	Electrical Engineering	4/97
Tsinghua University, Beijing, China	B. Eng.	Electronic Engineering	7/92

Professional Experience:

8/07 – present	Associate Professor, Department of Electrical and Computer Engineering, Southern Illinois University (SIU), Carbondale, IL 62901
8/02 – present	Assistant Professor, Department of Electrical and Computer Engineering, Southern Illinois University (SIU), Carbondale, IL 62901
1/97 – 5/02	Research Assistant, Department of Electrical and Computer Engineering, University of Arizona, Tucson, AZ 85721
5/00 – 8/00	Intern, Wireless Integration Technology Center, Motorola, Libertyville, IL 60030
6/98 – 8/98	Intern, Rockwell Semiconductor Systems, San Diego, CA 92121
9/96 – 12/96	IC Design Engineer, Siemens Components Pte. Ltd., Singapore, 349249
9/94 – 8/96	Research Assistant, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, 639798
9/92 – 8/94	Teaching Assistant, Institute of Microelectronics, Tsinghua University, Beijing, China

Honors and Awards:

- NSF CAREER award, 2005
- Best paper award, 8th International Symposium on Quality Electronic Design, San Jose, CA, 2007
- Outstanding paper award, 8th International Conference on Mixed Design of Integrated Circuits and Systems, Poland, 2001

Research Funding:

- Development and demonstration of an automation and control system for coal spiral, Illinois Department of Commerce and Economic Opportunity (IDCEO/ICCI), PI: Manoj Mohanty, Co-PI: Haibo Wang, $149,897, 01/10-05/11
- A Portable Medical Instrument for Objectively Diagnosing Human Tinnitus, SIU School of Medicine, Concept Development Award, PI: Jeremy Turner, Co-PI's: Jun Qin, Haibo Wang, $13,800, 08/09-05/10
- National Science Foundation, "CAREER: implementing mixed-signal circuits with self-testing and self-repairing capabilities," PI: Haibo Wang, $400,000, 03/05–02/10
- An Ultrasonic Tracking System for Motion Capture Studies in Ergonomic Applications, Caterpillar, Inc., PI: Ajay Mahajan, co-PI: Haibo Wang, Phase I: $39,995, 05/06-08/07; Phase II: $75,720, 09/07-12/08; Phase III: $95,031, 12/08-12/09

Professional Service:

- Technical Program Committee of 24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2009, Chicago, IL.
- Technical Program Committee of 2007-2010 International Symposium of Quality Electronic Design, San Jose, CA.
- Session Co-Chairs at 2007, 2008 International Symposium of Quality Electronic Design, San Jose, CA.
- Program Committee of 2003 International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland
- Session Chair of 2000 International Symposium on Circuits and Systems, Phoenix AZ.

Selected Publications:

1. B. Soewito, L. Vespa, A. Mahajan, N. Weng and H. Wang, "Self Addressable Memory-based FSM (SAM-FSM): A Scalable Intrusion Detection Engine," IEEE Network, vo. 23, no. 1, pp. 14 - 21, January, 2009
2. B. Soewito, A. Mahajan, N. Weng, and H. Wang, "High-speed String Matching for Network Intrusion Detection," Int. Journal of Communication Networks and Distributed Systems (IJCNDS), Vol. 3, No. 4, pp. 319-339, 2009.
3. A. Laknaur, R. Xiao, S. Durbha, and H. Wang, "Design of a Window Comparator with Adaptive Error Threshold for Online Testing Applications," Microelectronics Journal, Vol. 40, No. 9, pp. 1257-1263, 2009.
4. A. Laknaur, R. Xiao, S. Durbha, and H. Wang, "Design of a Window Comparator with Adaptive Error Threshold for Online Testing Applications," Proc. 8th International Symposium on Quality Electronic Design, San Jose, CA, March, 2007, pp.501-506.
5. M. Skoufis, H. Wang, T. Haniotakis, and S. Tragoudas, "Glitch Control with Dynamic Receiver Threshold Adjustment," Proc. of 8th International Symposium on Quality Electronic Design, San Jose, CA, 2007, pp. 410-415.
6. R. Zakeri, C. Watts, H. Wang, and P. Kohli, "Synthesis and Characterization of Non-linear Nanopores in Alumina Films," ACS Chemistry of Materials, Vol. 19, 2007, pp. 1954-1963.
7. A. Laknaur, S. Durbha, and H. Wang, "Built-in-Self-Testing Techniques for Programmable Capacitor Arrays," Journal of Electronic Testing: Theory and Applications, Vol. 22, No. 6, 2006, pp. 449-462.
8. S. Durbha, A. Laknaur, and H. Wang, "Investigating the efficiency of Integrator-Based Capacitor Array Testing Techniques," Proc. of 24th VLSI Test Symposium, Berkeley, CA, May, 2006, pp. 320-325
9. K. Raghuraman, H. Wang, and S. Tragoudas, "A Novel Approach to Minimizing Reconfiguration Cost for LUT-Based FPGAs," Proc. of 18th Intl. VLSI Design Conference, Jan. 2005, pp. 673 – 676.
10. Laknaur and H. Wang, "A Methodology to Perform Online Self-Testing for Field Programmable Analog Array Circuits," IEEE Trans. Instrumentation and Measurement, Vol. 54. No. 5, 2005, pp. 1739-1750.
11. H. Wang, S. Kulkarni, and S. Tragoudas, "On-line Testing Field Programmable Analog Array Circuits," Proc. of International Test Conference, 2004, Charlotte, NC, pp. 1340-1348.
12. H. Wang, S. Kulkarni, and S. Tragoudas, "Circuit Techniques for Field Programmable Analog Array On-line Testing," Proc. of 10th International Mixed-Signal Testing Workshop, June 2004, pp.237-244.
13. H. Wang and S. B. K. Vrudhula, "Behavioral Synthesis of Field Programmable Analog Array Circuits," ACM Trans. on Design Automation of Electronic Systems, Vol. 7, Oct. 2002, pp. 563-604.
14. H. Wang, S. B. K. Vrudhula, and O. A. Palusinski, "Performance Driven Placement and Routing for Field Programmable Analog Arrays," Proc. of the 8th International Conference on Mixed Design of Integrated Circuits and Systems, 2001, Poland, pp. 207-212.
15. H. Wang and P. C. Liu, "Double-Edge-Triggered Address Pointer for Low Power High Speed FIFO Memories", IEE Electronics Letters, Vol. 33, No. 5, February 1997, pp. 387-389.

SPYROS TRAGOUDAS

PROFESSIONAL AFFILIATION AND CONTACT INFORMATION

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EDUCATION

1986 Diploma (5 years), Computer Engineering and Informatics Department, University of Patras, Greece

1988 M.S., Erik Jonsson School of Engineering and Computer Science, Computer Science Program, The University of Texas at Dallas, Richardson, TX 75083-0688.

1991 Ph.D., Erik Johnson School of Engineering and Computer Science, Computer Science Program, The University of Texas at Dallas, Richardson, TX 75083-0688.

PROFESSIONAL EXPERIENCE

07/1/12- current Department Chair, Electrical & Computer Eng. Dept., Southern Illinois University Carbondale.

03/01/09-current Director, NSF IUCRC on Embedded Systems, SIUC-site.

07/16/99- current Professor, Electrical & Computer Eng. Dept., Southern Illinois University Carbondale.

08/16/98-07/15/99 Associate Professor, Electrical and Computer Engineering Department, The University of Arizona.

08/16/91-08/15/98 Associate Professor, Computer Science Department, Southern Illinois University Carbondale (in the rank of untenured Assistant Professor until 6/30/96).

07/01/97-08/15/98 Graduate Program Director, Computer Science Department, Southern Illinois University Carbondale.

01/03/87-08/14/91 Research/Teaching Assistant, Computer Science Program, School of Engineering and Computer Science, The University of Texas at Dallas, Richardson, TX 75083-0688.

08/15/86-01/02/87 Systems Analyst, Computer Technology Institute, Patras, Greece.

RESEARCH INTERESTS

Design and Test Automation for VLSI, Embedded Systems

RESEARCH SPONSORS

Direct support: National Science Foundation, US Navy, SAIC, Intel, Qualcomm, Synopsys

NSF IUCRC: NSF, NAVSEA Crane, SAIC, Intel, Caterpillar, Dickey-john, EMAC, Wildlife Materials

PROFESSIONAL SERVICE

Editorial Board: IEEE Transactions on Computers, VLSI Design journal, Universal Computer Science, Research Letters in Electronics.

General Chair of IEEE DFTS 2010, Program Committee Chair of DFTS 2009, Program Committee member of many International Conferences

Has graduated 14 PhD students and supervised over 60 MS theses. Currently advising 11 PhD students

PUBLICATIONS

Over 60 journal papers and over 100 articles in peer-reviewed conference proceedings

Ten recent journal publications

• A.K. Palaniswamy and S.Tragoudas, An Efficient Heuristic to Identify Threshold Logic Functions, ACM Journal on Emerging Technologies in Computing (JETC), to appear in 2012.

• M.N. Skoufis, S. Tragoudas, An on-line Failure Detection Method for Data Buses using Multi-threshold Receiving Logic, IEEE Transactions on Computers, vol. 61, no. 2, pp. 187-198, Feb. 2012

• K. Stewart, Th. Haniotakis, and S. Tragoudas, Securing sensor networks: A novel approach that combines encoding, uncorrelation, and node disjoint transmission, Ad Hoc Networks, vol. 10, issue 3, May 2012, pp. 328-328, Elsevier.

• M.N. Skoufis, K. Karmakar, S. Tragoudas, and T. Haniotakis, A data capturing method for buses on chip, IEEE Transactions on Circuits and Systems I, vol. 57, no. 7, pp.1631-1641, July 2010.

• D. Jayaraman, R. Sethuram, and S. Tragoudas, Scan Shift Power Reduction by Gating Internal Nodes. J. Low Power Electronics 6(2): 311-319 (2010).

• E. Flanigan, S, Tragoudas, Path Delay Measurement Techniques using Linear Dependency Relationships, IEEE Transactions on VLSI Systems, vol. 18, issue 6, pp.1011-1015, June 2010.

• R. Adapa, S. Tragoudas, Techniques to Prioritize Paths for Diagnosis, IEEE Transactions on VLSI Systems, vol. 18, issue 4, pp. 658-661, April 2010.

• K. Christou, M. K. Michael, and S. Tragoudas, On the Use of ZBDDs for Implicit and Compact Critical Path Delay Fault Test Generation, Journal of Electronic Testing: Theory and Applications, 2008.

• A. Abdulrahman and S. Tragoudas, Low-Power Multi-Core ATPG to Target Concurrency, Integration, the VLSI Design Journal, vol. 41, issue 4, pp. 459-473, July 2008.

• C. Song, S. Tragoudas, Identification of Critical Executable Paths at the Architectural Level, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), vol. 27, no. 12, pp. 2291-2302, December 2008.

I/UCRC Executive Summary - Project Synopsis		Date: 4/8/2013
Project Title: Adaptive compressive sensing techniques for low power sensors		
Center/Site: Center for Embedded Systems/Southern Illinois University		
Principle Investigator: Haibo Wang and Spyros Tragoudas		**Type: (New or Continuing)** Continuing
Tracking No.: (CES office to input)	**Phone :** (618) 453 - 1522 (618) 453 - 7645	**E-mail :** {haibo, Spyros}@engr.siu.edu
		Proposed Budget: $50,000

Abstract: (250 words max)
The objective of this project is to investigate novel adaptive approaches to more effectively apply compressive sensing (CS) techniques in low-power sensor systems. Recently, CS emerged as an attractive technique in low-power sensor development, because of its capability to allow sensor signals to be sampled at rates lowers than Nyquist rate. In CS method, the number of sampled compressive signals is selected according to the sparseness of the sensor signals. Currently, the majority of CS circuits use fixed sampling rates during the entire sensing operations. To further reduce the power consumption of sensors using compressive sensing, we have been investigating the potentials of adaptively adjusting the sampling rates used in compressive sensing methods at system level. As a natural extension to the current effort, the proposed research is to investigate circuit techniques to execute adaptive CS. Particularly, we will investigate the use of low-power analog wavelet transformation circuit to detect when sampling rate can be changed in adaptive CS.

Problem:
For a compressible sensor signal X (containing N sampled data points), which has K significant terms projected into domain Ψ. The required size (M) of the sampled compressive sensor output (Y) is $M = \mathrm{O}(K \log \frac{N}{K})$. Currently, most CS circuits are designed with fixed M values. However, if signal sparsity changes during sensor expected life cycle, this may result in different K values and hence it is desirable to use different M values. For CS circuits designed for fixed M values, such variations potentially degrade sensor performance in terms of either accuracy or power efficiency

Rationale / Approach:
We have been investigating the sparsity variations for signals collected by biomedical sensors. Our study indicates that signal sparsity varies over the time and at different operating conditions. We are also working on estimating the potential power saving if the sampling rate used in compressive sensors can be adaptively adjusted according to signal sparsity variations, which also indicates that adaptive CS is an attractive technique for further reducing power consumption of sensor nodes. An import question that needs to be answered in the implementation of adaptive CS is how to detect the signal sparsity changes and subsequently adjust the sampling rate. To tackle this question, the proposed research investigates the use of low-power analog wavelet transformation circuit to detect when sampling rate can be changed in adaptive CS. We will first develop a low-power analog wavelet transformation circuit using a 0.13μm CMOS technology. Circuit simulation will be performed with ECG and EEG signals as inputs. Through extensive circuit simulations, we aim to establish the relations between the analog WT circuit output and the sparsity of the signals. With the established relations, we will further investigate the effectiveness of using the analog WT circuit to determining the sampling rates in adaptive CS.

Novelty:
Compressive sensing is a relatively new approach to reduce the power consumption of certain type sensors. The proposed work helps make compressive sensing more power efficiency, hence advances the state of the art of compressive sensing.

Potential Member Company Benefits:
The developed techniques have the potentials to help member companies further reduce the power consumptions of certain sensor devices in productions or used in their research and development (R&D) projects.

Deliverables for the proposed year:
1. Design of the analog wavelet transformation circuit
2. Investigation results on the effectiveness of using analog wavelet transformation circuit to determine the sampling rates in adaptive compressive sensing

Milestones for the proposed year:
3. **Quarter 1 (08/13-10/13):** Finalize the structure and complete the key optimization issues for the circuit to be designed
4. **Quarter 2 (11/13-01/14):** Complete the circuit design
5. **Quarter 3 (02/13-04/13):** Establish the relation between circuit output and signal sparsity via extensive simulations
6. **Quarter 4 (05/13-07/14):** Investigate the effectiveness of the proposed approach

Progress to Date: THIS SECTION TO BE UPDATED IN JANUARY

Estimated Start Date: 8/1/2013	**Estimated Knowledge Transfer Date**: 7/30/2014