CES Research Report
Sothern Illinois University Carbondale
Arizona State University
Fundamental Research Project: Collaborative Research: Synthesis and Design of Robust Threshold Logic Circuits
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Project Description

Embedded systems, which have been widely used in various applications, will be rapidly evolved into many forms and ubiquitously deployed to improve virtually every aspect of human life and the society. A significant challenge in the path to this bright future is to develop high-performance and low-power System-on-a-Chip (SoC) devices, which are core components in every modern embedded system. This project tackles this challenge by developing both synthesis and circuit techniques that enable using Threshold Logic (TL) circuits to implement complex SoCs for high-performance and low-power embedded systems.

Recent research has demonstrated that TL circuits outperform conventional logic circuits for CMOS technologies and can serve as an excellent choice for implementing digital circuits using future nano devices. The proposed research develops effective TL circuit synthesis algorithms that simultaneously optimize power, area, speed, and robustness of the TL circuits. It develops analytical models and subsequently establishes systematic design and optimization procedures for TL gate design using both CMOS and future nano devices. It also explores new techniques to achieve post-fabrication configuration at the TL gate level to effectively cope with process variations and defects, which are expected to be worsen for future atomic-scale devices. Furthermore, the project investigates applying the developed TL circuit techniques in Time-to-Digital Converter (TDC) based Analog-to-Digital Converter (ADC) designs. Finally, the developed techniques will be evaluated using the benchmark circuits provided or suggested by member companies of the NSF IUCRC Center for Embedded Systems which have interests and expertise in embedded systems for a wide range of applications.

Objectives

The objectives of this research is to develop synthesis algorithms and circuit techniques that constitute a new TL circuit design flow, in which logic synthesis and transistor level circuit design can be closely interacted to effectively address the power, performance and process variation challenges. Additionally, the project will expand the application of TL circuit techniques into the mixed-signal domain by developing novel ADCs with using TL circuits.

Industrial Relevance

With the current device scaling trend, CMOS device feature size will be scaled down to 14nm and beyond in the very near future. SoCs implemented with such atomic-scale devices are expected to experience extreme variability in nearly all the circuit characteristics due to process variations and material defects at the atomic level. Such variability adversely affects the circuit performance improvement attributed by scaling. Meanwhile, device scaling alone is not adequate to address the power challenge due to the increased number of devices placed on the SoC chips and increased device leakage currents. The recent researches indicate that TL circuits have great potentials to become the enabling circuit techniques to address the power and performance challenges in current and future nano-meter CMOS technologies, and to serve as an excellent choice for implementing digital circuits for post-CMOS devices in the long term.

Project Outcomes

The project develops effective TL synthesis, TL gate optimization, TL circuit testing techniques for achieving robust TL circuits, and approaches to extend TL circuit techniques to the design of successive approximation register (SAR) analog to digital converter (ADC) circuits. Specifically, the project outcomes are:

1. The research efforts on TL synthesis resulted in two improved TL synthesis approaches: one is based on implicant-implicit algorithms and the other is for nanopipelined TL circuit thesis. These two approaches are described in two journal publication [1, 2].
2. The research efforts on TL gate optimization led to an accurate gate delay formula, which is reported on a conference paper [3]; gate delay optimization procedures are established based on the TL delay formula. In addition, a novel low-power high-speed memristor-based TL gate design is developed and presented in a conference paper [4].
3. The research on TL gate testing developed two automatic test pattern generation (ATPG) methods for transistor faults on current-mode TL circuits. The developed method is able to sensitize the pattern sensitive transition fault with the maximum possible delay. The preliminary results are presented in a conference paper [5].
4. The research on TL-inspired ADC design led a new SAR ADC topology, which is referred to as accelerated successive approximation register (A-SAR) ADC. The preliminary result has been accepted for a conference presentation [6] and won a best paper award.

Research Team

The research team comprise of Drs. Spyros Tragoudas, Sarma Vrudhula, and Haibo Wang. Drs. Tragoudas and Wang are with SIU and Dr. Vrudhula is with ASU.

References

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