Center for Embedded Systems

An NSF Industry/University Cooperative Research Center

State of the Center

Sarma Vrudhula, Arizona State University

Spyros Tragoudas, Southern Illinois University, Carbondale

Industrial Advisory Board meeting

June 12-13, 2012

SIU Southern Illinois University Carbondale

National Science Foundation

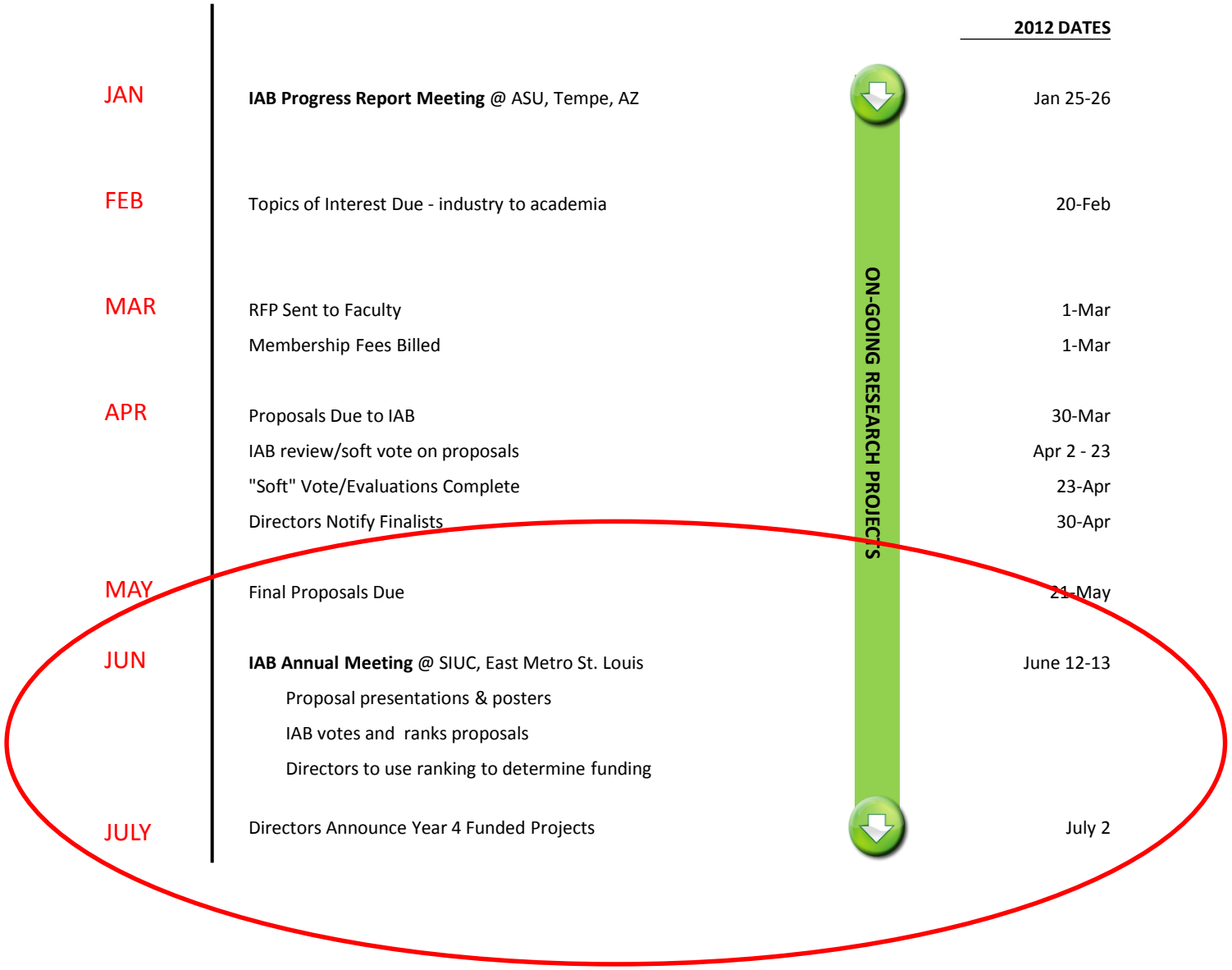
ASU Ira A. Fulton Schools of Engineering

Arizona State University

Thank You

- Nancy Beasley, CES Project Manager at SIU
- Lisa Christian, CES Project Manager at ASU
- Spyros Tragoudas – SIU Site Director

Project Selection Process



Industry Membership

	Year 1	Year 2	Year 3	Year 4
Intel (AZ)	✔	✔	✔	✔
Raytheon	✔	✔	✔	✔
Intel (OR)	✔	✔	✔	✔
NAVSEA Crane	✔	✔	✔	
Wildlife Materials	✔	✔		
EMAC		✔	✔	
Intel (CA)		✔	✔	✔
Caterpillar		✔	✔	✔
Qualcomm		✔	✔	✔
Toyota		✔	✔	✔
DICKEY-john		✔	✔	✔
Marvell			✔	✔
General Dynamics			✔	✔
Hamilton Sundstrand			✔	✔
Rockwell Collins				✔

ASU and SIU Participants

Year 1:

8 Faculty

14 Graduate Students

10 Projects

45 Internships (Intel Az)

Year 2:

12 Faculty

19 Graduate Students

15 Projects

30 Internships (Intel Az)

Year 3:

15 Faculty

30 Graduate Students

16 Projects

35 Internships (Intel Az)

Year 4:

21 Projects proposed

19 Faculty involved

Recruiting Efforts

National Instruments	Georgios Fainekos
Freescale	Karam Chatha, Sarma Vrudhula
AFOSR	Hugh Barnaby, Sarma Vrudhula
Texas Instruments	Aviral Shrivastava
Cisco	Aviral Shrivastava
Qualcomm Research	Hugh Barnaby, Michael Kozicki, Sarma Vrudhula
Xilinx, Intel Labs	Karam Chatha

Technology Transfer

"As promised in our first research proposal, we were able to use ASU Professor Fainekos' S-TaLiRo Tool suite prior to physical engine testing to expose performance specification violations in one of our research controller designs. Thus, we conclude that the tool suite can be incorporated to improve our control design process. We look forward to similar success in our second project wherein we will study the effective use of multi-core processors in engine control applications." – Ken Butts, Executive Engineer, Toyota Motor Engineering & Manufacturing, N.A., Ann Arbor, MI

"The NSF Center for Embedded Systems has enabled us to integrate network-on-chip synthesis technologies developed by Professor Chatha's group into Qualcomm Corp R&D design processes. Our interaction has been very good, and we have also had the benefit of attracting technically strong interns." - Rudy Beraha, Director, Engineering, Qualcomm Corp., San Diego, CA

Year 3 Projects - SIUC

Year	Title	Faculty
3	Distance Estimation to a Transmitter With a Secure Network of Receivers	Spyros Tragoudas, Khadija Stewart
3	Statistical Fault Grading and Diagnosis	Spyros Tragoudas
3	Development of Fast Grain Quality Measurement System	Ying (Ada) Chen, Jun Qin
3	Survey and Assessment of Advanced Haptics Technology	Jun Qin
3	JTAG-Based Device Security for Embedded System	Spyros Tragoudas, Ning Weng
3	Platform for Automated Test and Programming of Embedded System on Module	Spyros Tragoudas, Haibo Wang
3	Enhancing Embedded Systems Curriculum using Atom-based Platform	Ning Weng, Haibo Wang
3	Feasibility Study in Improving the reliability of an MSP430 Embedded System	Spyros Tragoudas
3	Towards Optimal Design of Networking Infrastructure in Bus-based Systems	Dimitri Kagaris, Harini Ramarpasad
3	Numerical Modeling of Coupled Thermo-Mechanical Processes	Shaikh Ahmed, Jun Qin, Philip Chu
3	System Verification Through the Temporal Correctness of its Embedded Cores	Spyros Tragoudas

Year 3 Projects - ASU

Year	Title	Faculty
3	A Light-Weight Runtime Multi-Tasking Scheduler for Embedded Multi-Core Architectures	Karam Chatha
3	Statistical Techniques for Property Exploration of Cyber-Physical Systems	Georgios Fainekos
3	Feasibility of Integrating Memristors & Threshold Logic for Compact, Low Power Digital Circuits	Hugh Barnaby Sarma Vrudhula,
3	Improving Usability of Multi-core DSPs with SPM (formerly Programming Non-coherent Cache Architectures)	Aviral Shrivastava
3	Replay-based Program Profiling & Analysis for Embedded Systems	Yann-Hang Lee

Year 4 Proposed Projects

	LIFE	Title	Faculty	School
1	1.1	Temporal Logic Testing for Stochastic Cyber-physical SystemS	Fainekos	ASU
2	1.2	Trustable Access Mechanisms for Embedded Systems	Weng, Tragoudas	SIUC
3	1.3	Parallelization of Embedded Control Applications on Multi-core Architectures: A Case Study	Fainekos, Chatha	ASU
4	1.4	Pilot Study of Energy Harvesting Devices towards the Development of a Prototype	Hatziadoniu, Harackiewicz, Chu	SIUC
5	1.5	Critical Path Analysis of Multicore Systems using BDDs	Tragoudas	SIUC
6	1.6	Improving Usability of Mulit-core DSPs with Scratch Pad Memories	Shrivastava	ASU
7	1.7	Survey and Assessment of Smart Materials for Haptics Applications	Qin	SIUC
8	1.8	All-optical Embedded Fiber-optic Up/down-links for Motor Controller	Sayeh	SIUC
9	2.1	Resolver Sensor Conditioning Size Reduction	Hatziadoniu, Wang	SIUC
10	2.2	Feasibility of Integrating Memristors and Threshold Logic for Compact, Low Power Digital Circuits	Barnaby, Vrudhula	ASU

Year 4 Proposed Projects

	LIFE	Title	Faculty	School
11	2.3	Adaptive Compressive Sensing Techniques for Low Power Sensors	Wang, Tragoudas	SIUC
12	2.4	Curriculum Development: Embedded System Design using Atom-based Platforms	Wang, Weng	SIUC
13	2.5	Development of Electronic System-level Harware-Software Co-synthesis Approach	Chatha	ASU
14	2.6	Towards Predictable Execution of Safety Critical Tasks on Mixed-Criticality Multi-Core Platforms	Ramaprasad, Kagaris	SIUC
15	2.7	Object Identification and Tracking Embedded for Embedded Systems	Gupta	SIUC
16	3.1	High Quality Power-Aware Testing Methodologies for Integrated Circuits	Tragoudas	SIUC
17	3.2	Design of an Optimal Closed Loop Controller and its Implementation in an OS Scheduler for Dynamic Energy Management in Heterogeneous Multi-Core Processors	Vrudhula	ASU
18	3.3	Ultra-low Power Sensor Wake-up Techniques,	Wang, Tragoudas	SIUC
19	3.4	Augmented Virtualization for Real-time Embedded Systems	Lee	ASU
20	3.5	Development of Fast Grain Quality Measurement System (Phase III)	Chen	SIUC
21	3.6	The Fundamental Research Project (FRP)	Tragoudas, Vrudhula, Wang	ASU/ SIUC

Agenda

TUESDAY, JUNE 12, 2012	
7:00 – 7:30 am	Registration Check-in and Breakfast, Drury Inn Breakfast Room
7:30 – 7:50 am	Opening Remarks & Introductions, Drury Inn Conference Room, Spyros Tragoudas (SIUC), Sarma Vrudhula (ASU), and John Warwick (CoE Dean, SIUC)
7:50 – 8:30 am	NSF Message, Rita Rodriguez, CISE Program Director, NSF CISE/CNS and Alex Schwarzkopf, NSF ENG/OAD
8:30 – 9:50 am	New Projects, year 4 – group 1 (1.1 - 1.8); 8 min presentations + LIFE forms
9:50 – 10:35 am	Poster Session, year 4 new projects – group 1
10:35 – 11:00 am	LIFE Forms Feedback: Discussion, year 4 new projects – group 1
11:00 am – 12:00 pm	Lunch / Break
12:00 pm	Reconvene
12:00 – 1:10 pm	New Projects, year 4 – group 2 (2.1 - 2.7); 8 min presentations + LIFE forms
1:10 – 1:55 pm	Poster Session, year 4 new projects – group 2
1:55 – 2:15 pm	LIFE Forms Feedback: Discussion, year 4 new projects – group 2
2:15 – 2:45 pm	Break
2:45 – 3:45 pm	New Projects, year 4 – group 3 (3.1 – 3.6); 8 min presentations + LIFE forms
3:45 – 4:30 pm	Poster Session, year 4 new projects – group 3
4:30 – 4:50 pm	LIFE Forms Feedback: Discussion, year 4 new projects – group 3
5:30 – 6:30 pm	Happy Hour (all), Drury Inn
6:45 pm	Dinner (all), Olive Garden, 25 Ludwig Drive, Fairview Heights, IL
WEDNESDAY, JUNE 13, 2012	
7:00 – 7:30 am	Breakfast, Drury Inn
8:00 – 11:00 am	IAB meeting (closed session), Drury Inn Conference Room