RECENT PROGRESS AND FUTURE PROSPECTS FOR MAGNETORESISTIVE RAM TECHNOLOGY

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EVERSPIN TECHNOLOGIES
The MRAM Company

Center for Embedded Systems IAB Meeting
Chandler, Arizona, 22 Jan 2013

Outline

- **MRAM overview**
- **Field-switched MRAM: “Classical Spintronics”**
- **Spin-torque MRAM: Spin-Torque-Transfer Spintronics**
- **Critical device properties and effect of materials**
- **Status: Fully-functional 64Mb, DDR3 ST-MRAM**
- **Summary**

Everspin – The MRAM Company

- **MRAM - Magnetic Random Access Memory**
  - *Fastest non-volatile memory with unlimited endurance*
- **Only company to have commercialized MRAM**
- **Founded 2008, 100%+ annual revenue growth**
- **Fundamental & essential MRAM IP**
  - *200+ US patents granted, 600+ WW patents & applications*
- **Backed by top-tier VC firms**

NewVenture Partners LLC

venturing beyond technology

SIGMA + PARTNERS

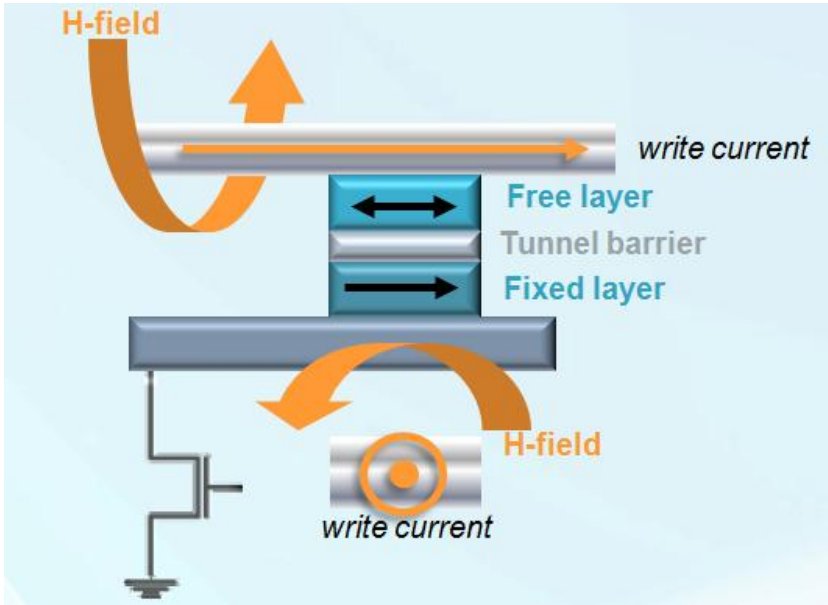
luxcapital

DRAPER FISHER JURVETSON

EPIC VENTURES

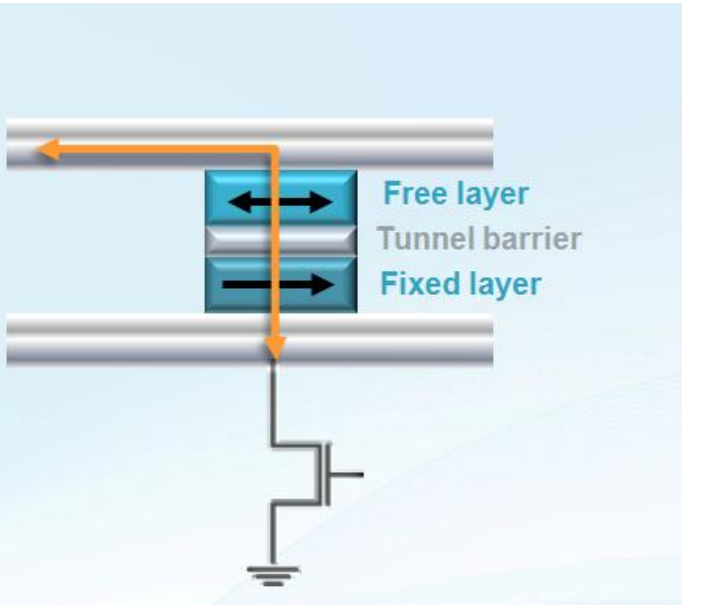
MRAM - Technology Comparison

Toggle Write



- Write with magnetic fields from current-carrying lines.
- High-performance, nonvolatile, unlimited endurance
- AlOx / NiFe-based MTJ
- In volume production

Spin-Torque Write



- Write with spin polarized current passing through the MTJ.
- Lower write current enables higher memory density
- MgO / CoFeB-based MTJ
- 64Mb sampling to customers

EVERSPIN TECHNOLOGIES
The MRAM Company

Everspin Toggle MRAM Attributes

Parameter	Capability
Non-volatile capability	• Data retention >20 years
Performance	• Symmetric read/write – 35ns
Endurance	• Unlimited cycling endurance
CMOS integration	• Easily integrates in manufacturing back-end • Compatible with embedded designs • No impact on CMOS device performance
Temperature range, reliability	• -40ºC < T < 150ºC operation demonstrated • Intrinsic reliability > 20 years lifetime at 125ºC
Soft error immunity	• MRAM cell radiation tolerant • Soft error rate from alpha radiation too low to measure (<0.1 FIT/Mb)
Environmentally friendly	• No battery, RoHS compliant, low power

MRAM Market Segments

	MRAM benefits
 **Storage & Server** • RAID, NAS, SAN & DAS Storage • Rack & Blade Servers	Better Reliability Fast Power Off/On No Batteries/Caps Lower TCO
 **Energy & Infrastructure** Single-Board Computer, Routers, POS, Gaming SmartGrid, SmartMeter, Solar, Wind …	Better Reliability Industrial Temp No Batteries/Caps Lower TCO
 **Automotive and Transportation** • Power Train, Brakes, Safety, Data Logging • MultiMedia, Navigation, Camera, Black Box	Better Reliability Automotive Temp Endurance Lower TCO

Current MRAM products

All Based on Toggle Switching

16-bit I/O		
Part Number	**Density**	**Configuration**
MR4A16B	16Mb	1Mx16
MR2A16A	4Mb	256Kx16
MR0A16A	1Mb	64Kx16

8-bit I/O		
Part Number	**Density**	**Configuration**
MR4A08B	16Mb	2Mx8
MR2A08A	4Mb	512Kx8
MR0A08B	1Mb	128Kx8
MR256A08B	256Kb	32kX8
MR0D08B	1Mb	128KX8, 1.8v I/O
MR256D08	256Kb	32KbX8, 1.8v I/O

SPI I/O		
Part Number	**Density**	**Configuration**
MR25H40	4Mb	512Kx8
MR25H10	1Mb	128Kx8
MR25H256	256Kb	32Kx8

48-BGA

- x8 Asynchronous parallel I/O
- x16 Asynchronous parallel I/O
- x8 Asynchronous parallel 1.8V I/O

44-TSOPII, 54-TSOP

- x8 Asynchronous parallel I/O
- x16 Asynchronous parallel I/O

8-DFN

- SPI-compatible serial I/O
- 40 MHz; No write delay

32-SOIC

- x8 Asynchronous parallel I/O

Extended	**-40 to +105 ºC**
Automotive	**-40 to +125 ºC**

Commercial	**0 to +70 ºC**
Industrial	**-40 to +85 ºC**

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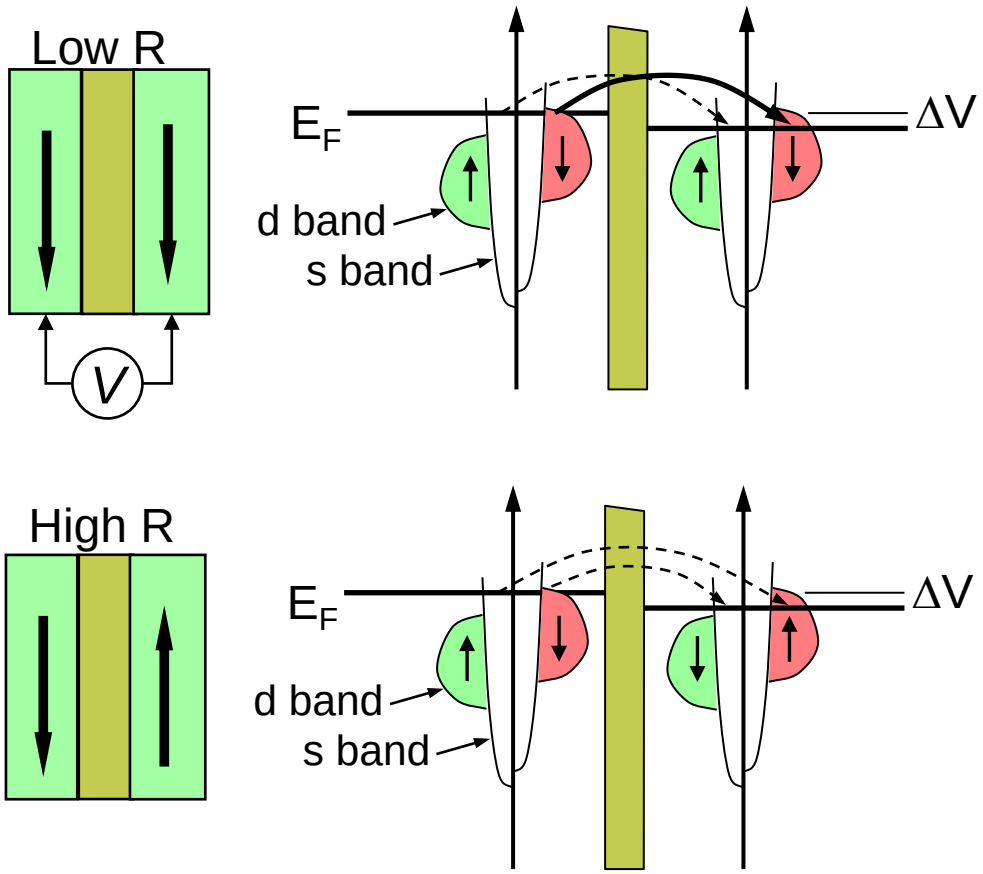
Tunneling Magnetoresistance

The tunneling is spin-dependent:
spin-up and spin-down have different probabilities.



First MTJ material with MR>10%: AlOx based in 1995

- Miyazaki & Tezuka, JMMM 139
- Moodera, et al. PRL 74

First MTJ material with MR~200% in 2004

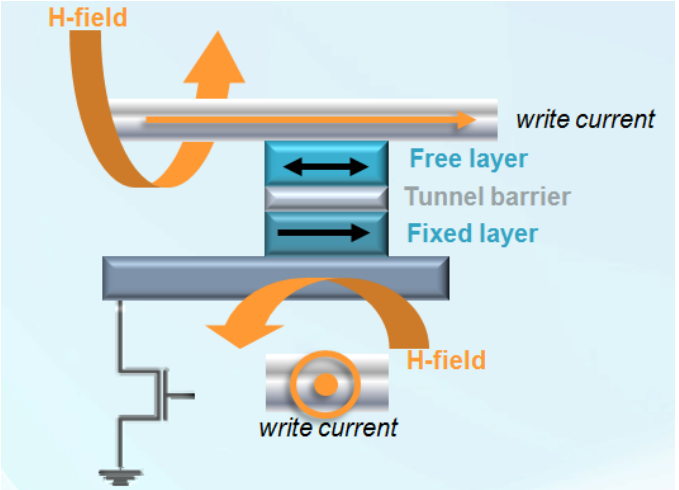
- Parkin, et al., Nat. Mat. 10.1038
- Yuasa, et al., Nat. Mat. 10.1038

$$MR = \Delta R / R_{low}$$

$$MR \sim 2P_1 \bullet P_2 / (1 - P_1 \bullet P_2)$$

Discovery to Commercial Application: TMR

- **Magnetic Tunnel Junctions with high Tunneling Magnetoresistance in 1995* led to first commercial MRAM in 2006+**
  - Tunneling resistance can be matched to CMOS transistors
  - Also used in HDD sensors



*J.S. Moodera, et al., PRL 74, 1995
*T. Miyazaki and N. Tezuka, JMMM 139, 1995
+ Freescale/Everspin 4Mb Toggle MRAM

Discovery to Commercial Application: STT

- **Two major developments spurred the second wave of MRAM development**
  1. Spin-torque demonstrations
  - M. Tsoi, et al. 1998 and J.A. Katine, et al. 2000
  2. MTJ material with MR~200%
  - Parkin, et al. and Yuasa, et al. 2004
- **Technology Demonstrations Include**
  - M. Hosomi, et al., IEDM 2005
  - R. Beach, et al. and T. Kishi, et al., IEDM 2008
  - S. Chung, et al. and D. C. Worledge, et al., IEDM 2010
  - W. Kim, et al., IEDM 2011
- **First Product Sampling: Everspin 64Mb 2012**

Recent Progress in Magnetic Switching

- **MgO/CoFeB-based MTJs with perpendicular magnetization**
  - S. Ikeda et al., (2010)
  - D.C. Worledge, et al., (2011)
  - Very active area of R&D worldwide
- **Other recent discoveries show potential for continued rapid improvement**
  - Voltage-controlled interface anisotropy
  - Voltage-controlled magnetism
  - Spin Hall effect

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1 T-1 MTJ MRAM Write Operation

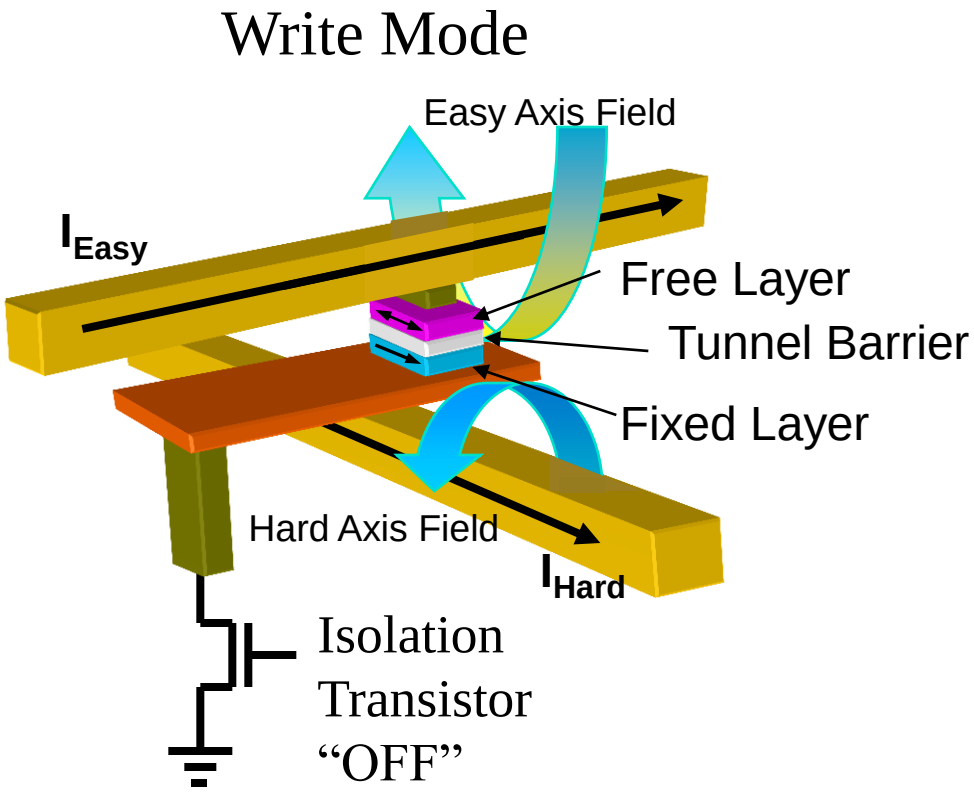
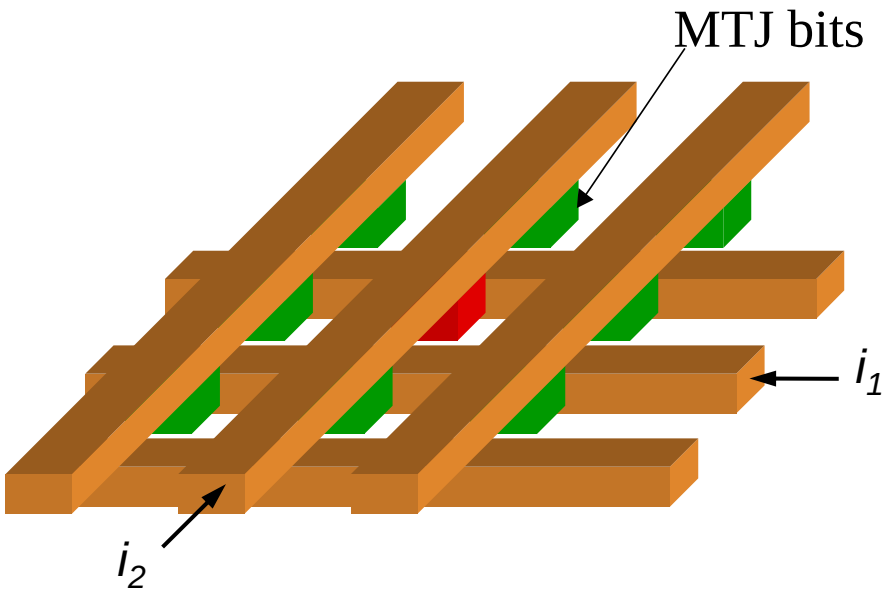
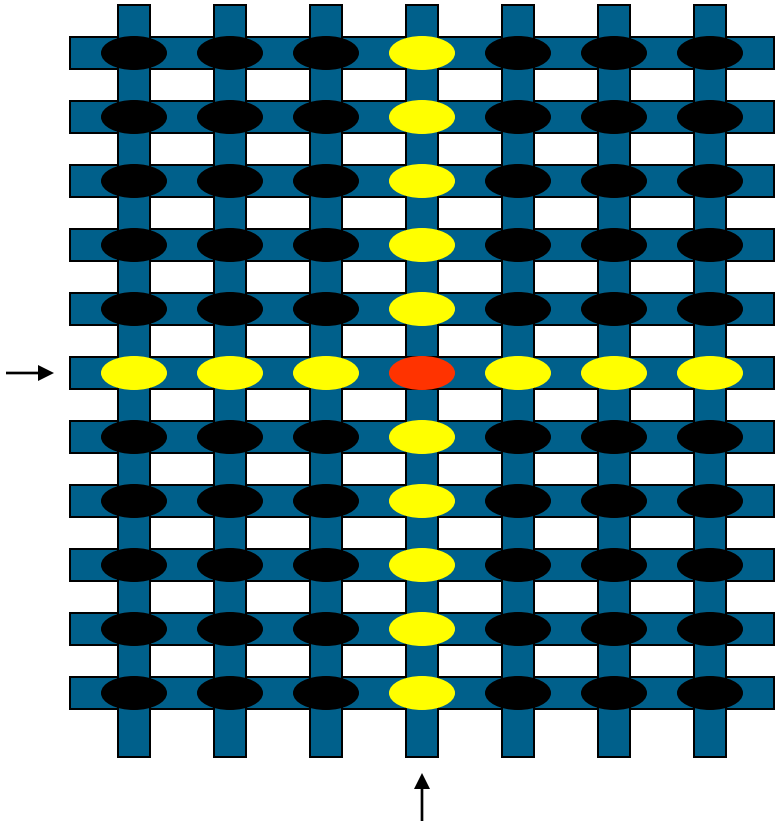


Figure 4



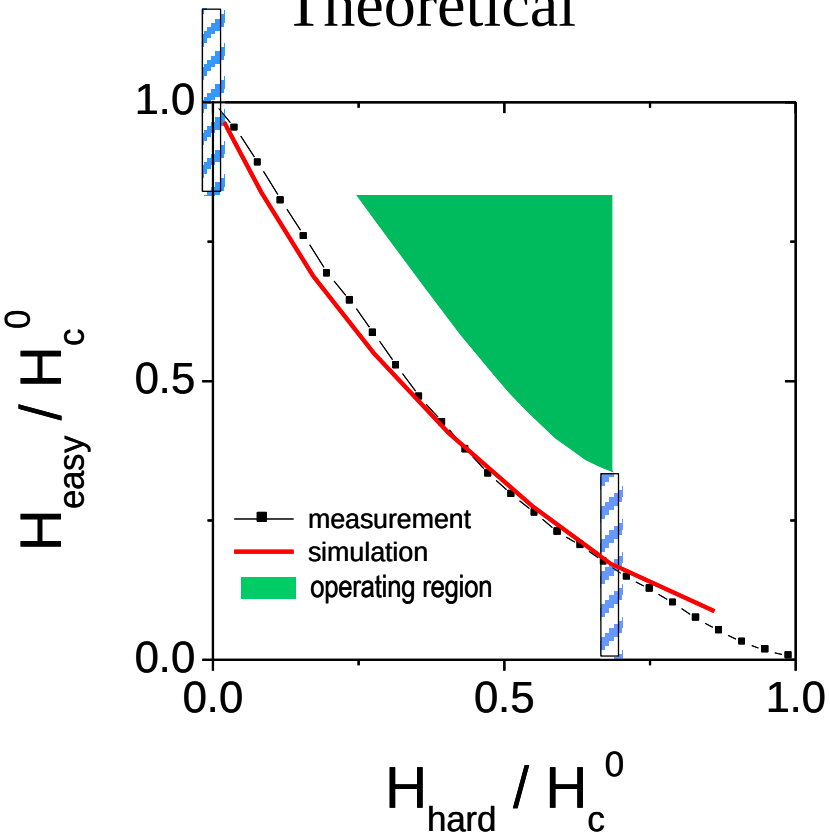
Conventional MRAM Bit Selection

- **Bit disturb margin**
  - Need many sigma separation between unselected and ½-selected distributions
  - All bits along selected current lines have reduced energy barrier during programming
    - Susceptible to disturb from thermal agitation

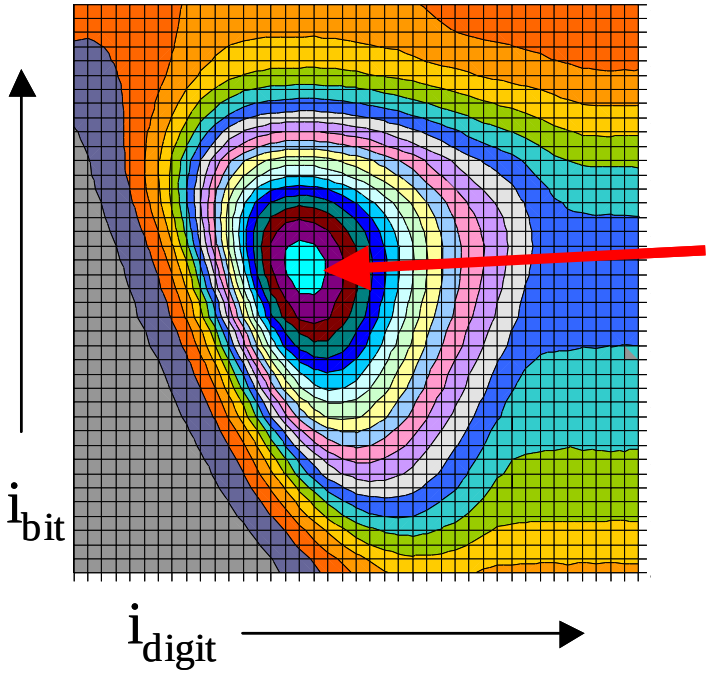


Conventional Operating Region

Theoretical

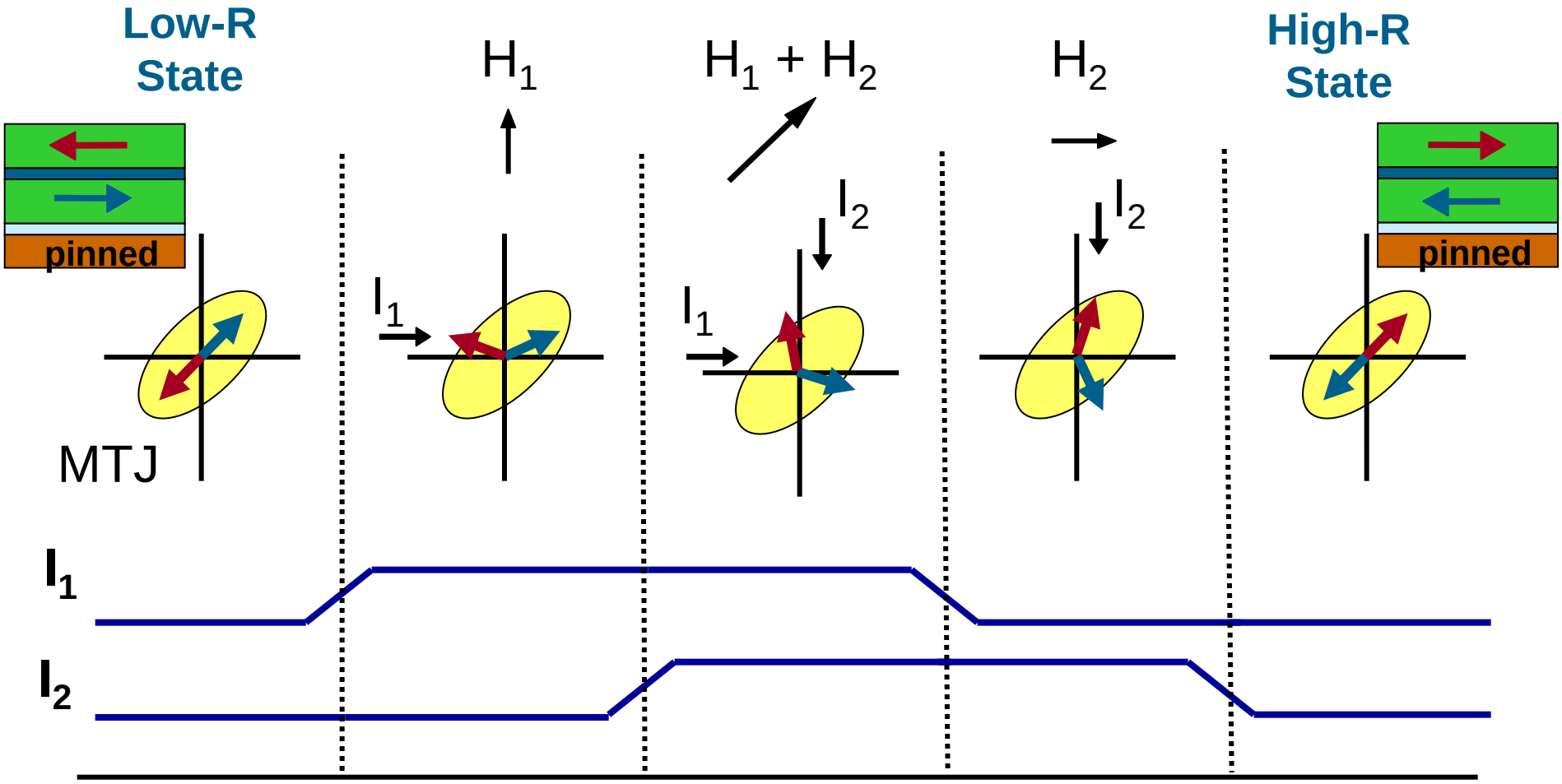


Experimental from 256k



- Challenge: Programming window sits between 2 distributions.
- Challenge: Thermal activation shrinks the window.

Toggle Write Operation

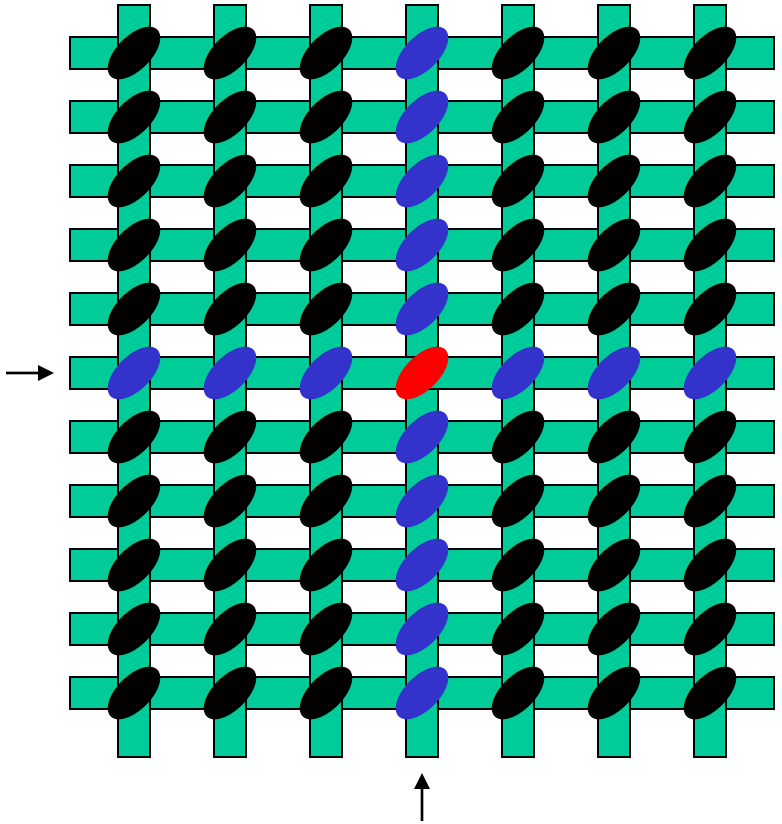


Advantages: Eliminates disturb - Large operating window

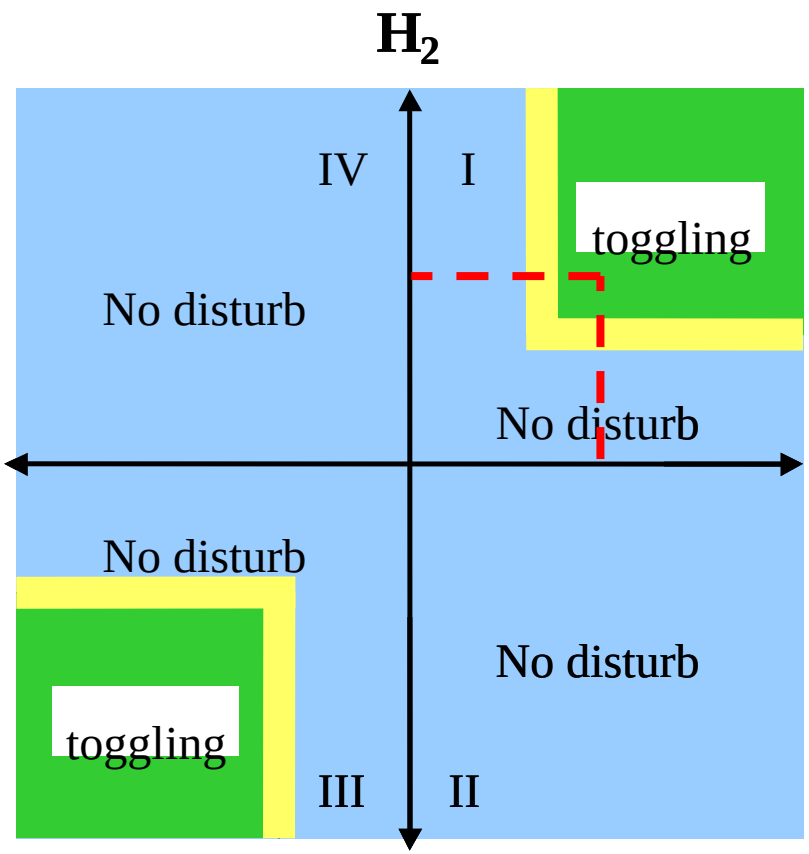
US Patent 6,545,906, Savtchenko et al. (2003)

Toggle-Bit Selection

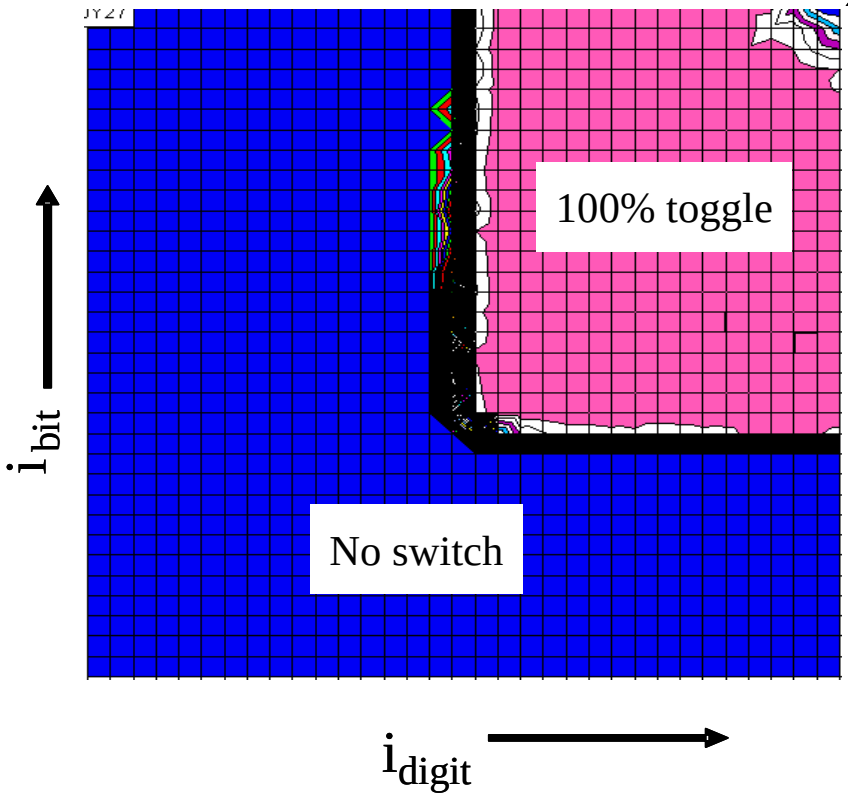
- **High bit disturb margin**
- **All bits along ½-selected current lines have increased energy barrier during programming**



Toggle-bit Array Characteristics



Switching map for a 4Mb
Toggle MRAM circuit



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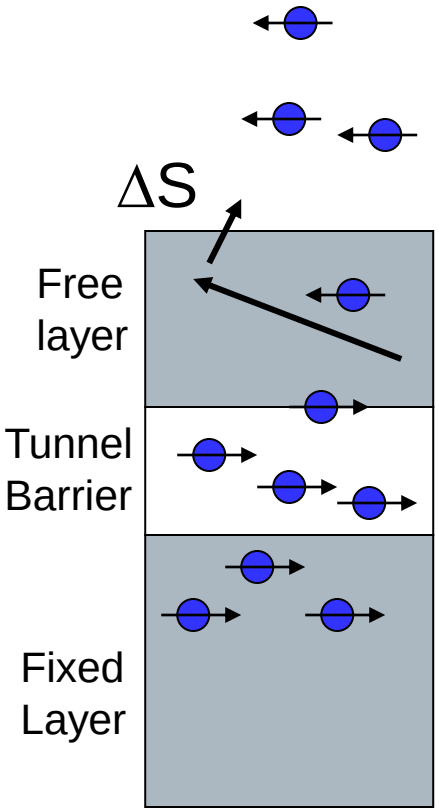
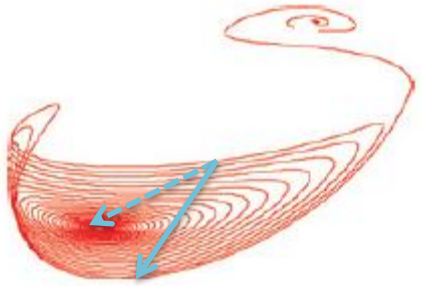
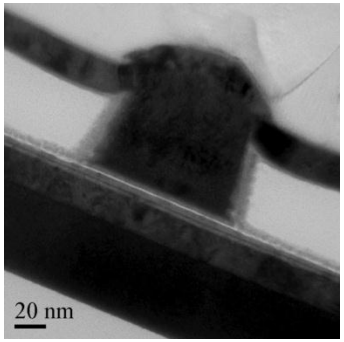
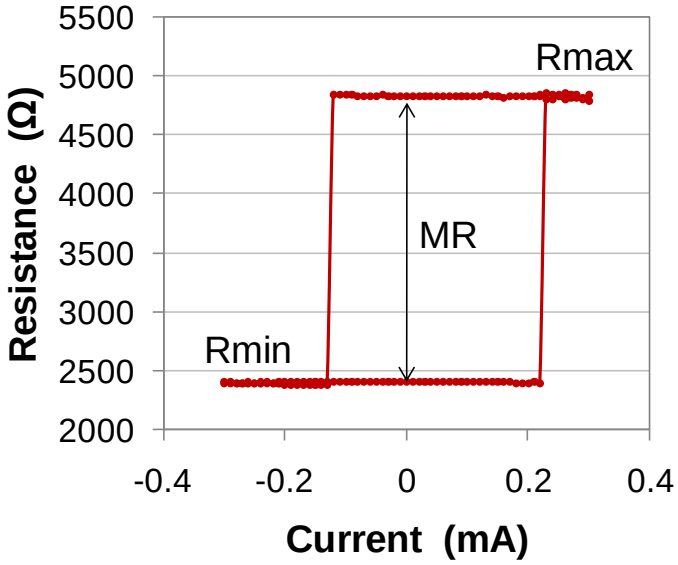
Spin-Torque MRAM

Use spin momentum from current to change direction of *S*, *m*.







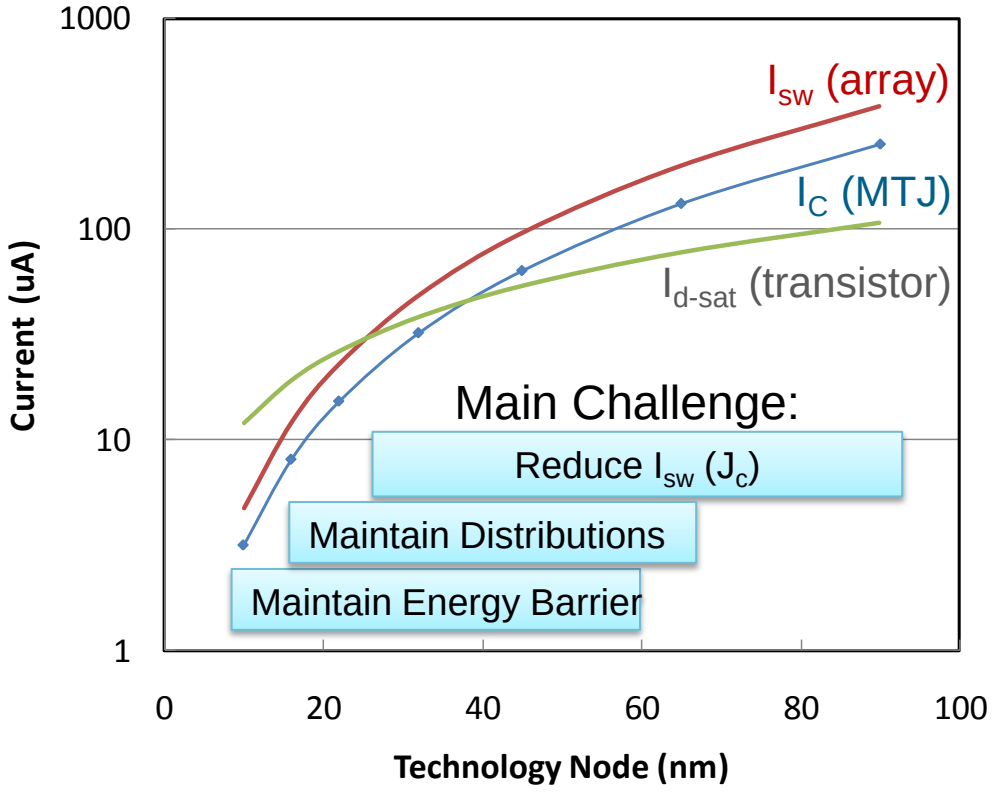


$$\frac{\Delta S}{\Delta t} = Torque$$

Need low resistance tunnel barrier to pass the required large current density, Jc > 1 MA/cm^2

Desired Scaling of Switching Current

- **Today: Reduce Jc for reliability and smaller transistors**
- **Continued scaling: maintain energy barrier and manage distributions while reducing Jc**



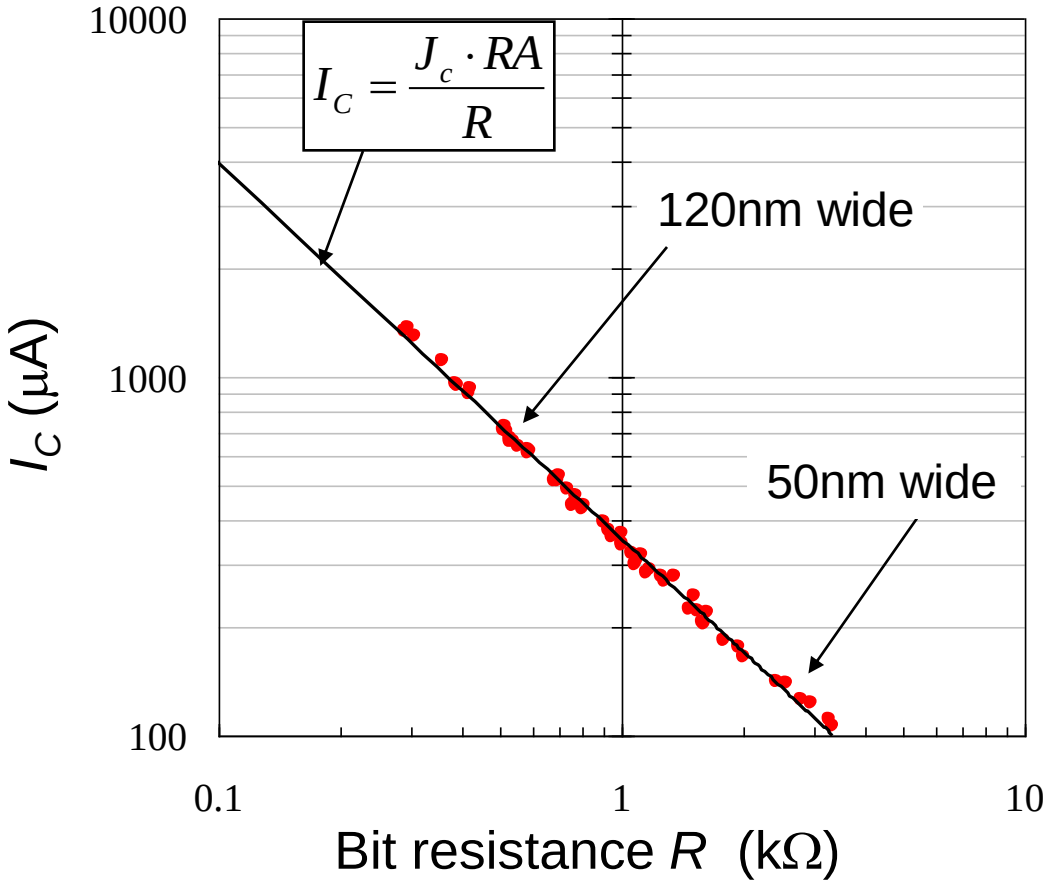
Scaling should maintain or reduce Jc, then:

- I_C scales favorably to transistor current

Maintain Eb/kT for non-volatility and control distributions

I_c calculated for J_c=2MA/cm^2

I_C scaling with bit size



$I_c \propto$ Area ⇒
$J_c \approx$ constant over range of bit sizes

- Data points = Ic for different bit sizes

- Bit width: 120nm →50nm
- Aspect ratio: 1.7 → 3.5

But need to maintain energy barrier for non-volatility!

Paths to lower I_c

- **For in-plane magnetization:**

$$I_C = \left(\frac{2e}{\hbar}\right)\left(\frac{\alpha M_s V}{\eta}\right)(H_k + 2\pi M_s)$$

Lower damping (α) free layer material

Increase spin-torque efficiency η

Lower M_s and/or thinner free layer **(E_b limited)**

Compensate for thin-film demagnetization field with PMA

See for example, Katine & Fullerton, Journal of Magnetism and Magnetic Materials 320 (2008) 1217–1226

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Ic with Perpendicular Magnetization

Bit shape

Thin-film demagnetization term

$$I_c = \frac{2e}{\hbar} \cdot \frac{\alpha MV}{\eta} \left(H_k^{in-plane} + 2\pi M_s - H_\perp / 2 \right)$$

Material with large perpendicular anisotropy can offset the demag. field

- **Two cases:**
  1. $H_\perp < 4\pi M_s$, in-plane with perpendicular assist
     - Energy barrier to reversal dominated by bit shape
  2. $H_\perp > 4\pi M_s$, perpendicular magnetization
     - Energy barrier to reversal dominated by $H_\perp$
     - Ic ~ Energy Barrier

Reduced In-Plane Ic with Perpendicular Assist

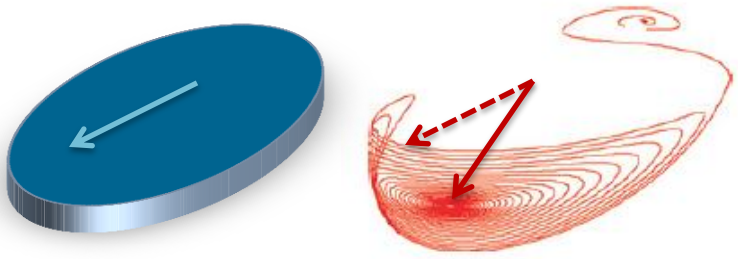
Bit shape

Large demagnetization term dominates I_c

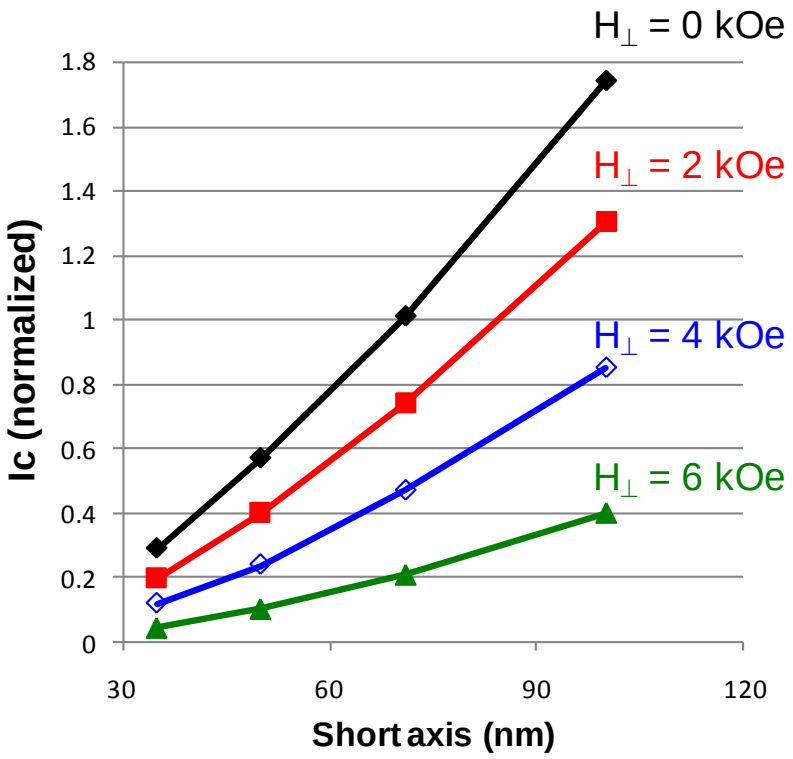
$$I_c = \frac{2e}{\hbar} \cdot \frac{\alpha MV}{\eta}\left(H_k^{in-plane} + 2\pi M_s - H_\perp/2\right)$$

Material with large perpendicular anisotropy can offset the demag. field

Moment must tilt out of plane during switching, but energy used to overcome demag. field is wasted

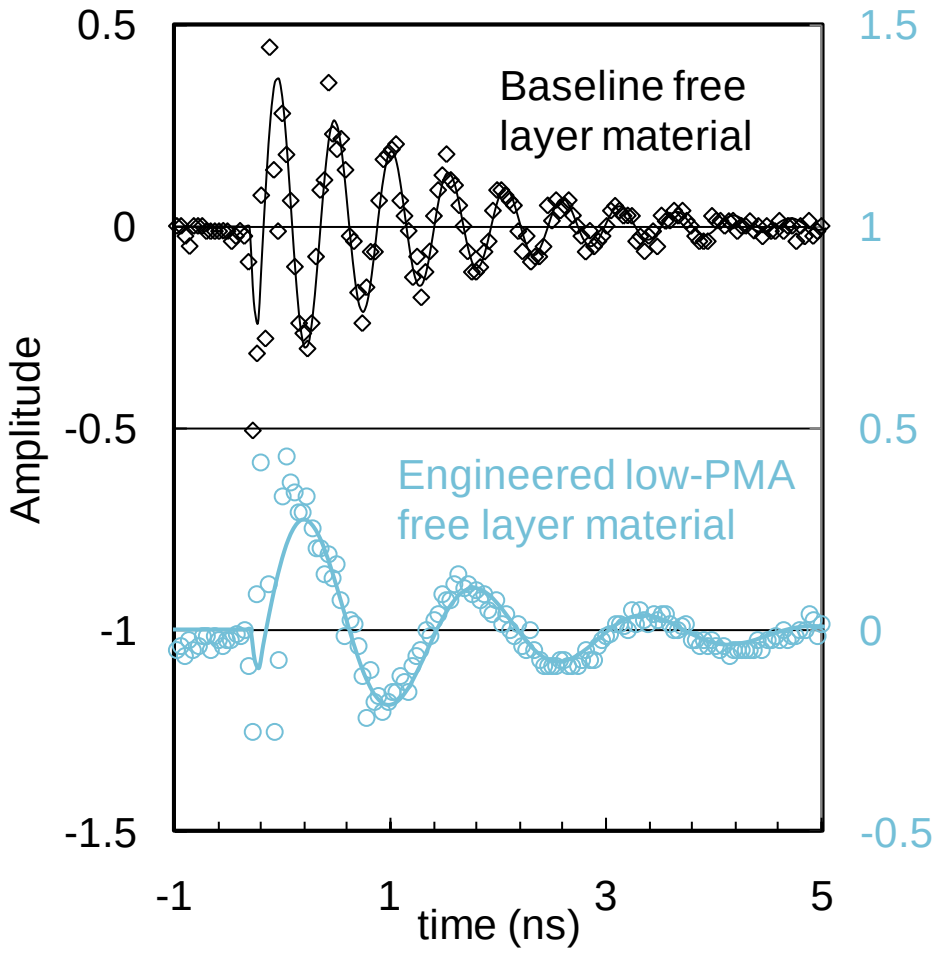


Magnetic Modeling Results



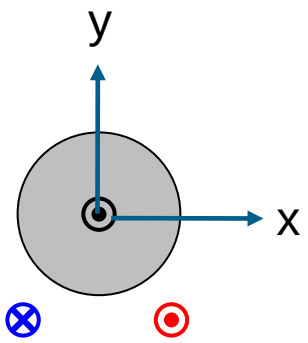
For bits with: AR=2, $4\pi M$=8kOe, E_b/kT=52

Engineered materials for Low J_c



- **Pulsed Permeameter measurements show magnetic oscillations in the material**
- **Low frequency indicates low perpendicular anisotropy**
- **Decay rate of oscillation shows magnitude of damping**

Scaling Perpendicular ST-MRAM Devices



- **Advantages over in-plane devices**
  - E_b depends on crystalline or interface anisotropy, not shape
  - Circular bits may allow decreased cell size
  - Materials with large $H_\perp$ enable acceptable E_b for very small bits
- **Remaining challenges for perpendicular devices**

$$I_c \propto MV\left(H_\perp - 4\pi M\right)$$

$$E_b = MV\left(H_\perp - 4\pi M\right)/2$$

  - $I_c \propto E_b \Rightarrow$ current does not scale if E_b is maintained
    - Need further improvements to continue scaling, such as very low damping

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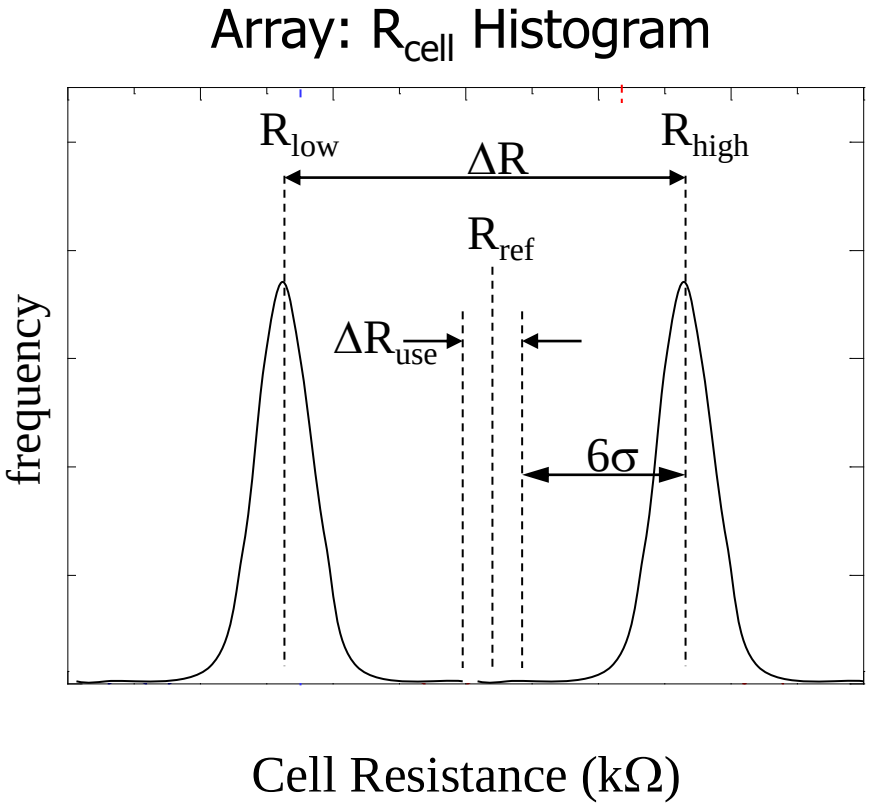
Magnetoresistance Signal and Distributions

$MR = \Delta R/R_{low}$, $\Delta R = R_{high} - R_{low}$

- **Signal = $R_{cell} - R_{ref}$**
  - ½ of ΔR available for sensing
- **Circuit works at finite bias**
  - MR is reduced by bias dependence of MR
- **Must sense all bits in the array**
  - Circuit must work with bits in tails of the R distribution



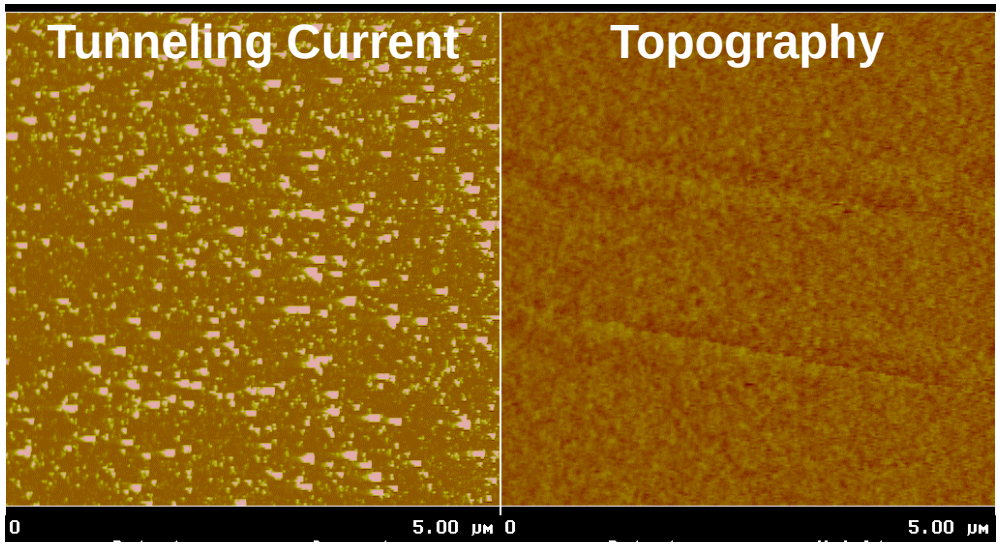
Resistance distribution reduces useable MR.

For six-sigma yield in the array, need: $\Delta R/2 > 6\sigma$

Uniformity of Tunneling Current Density

- **Tunneling current density has tunneling "hot spots"**
  - Result is statistical variation in bit resistance

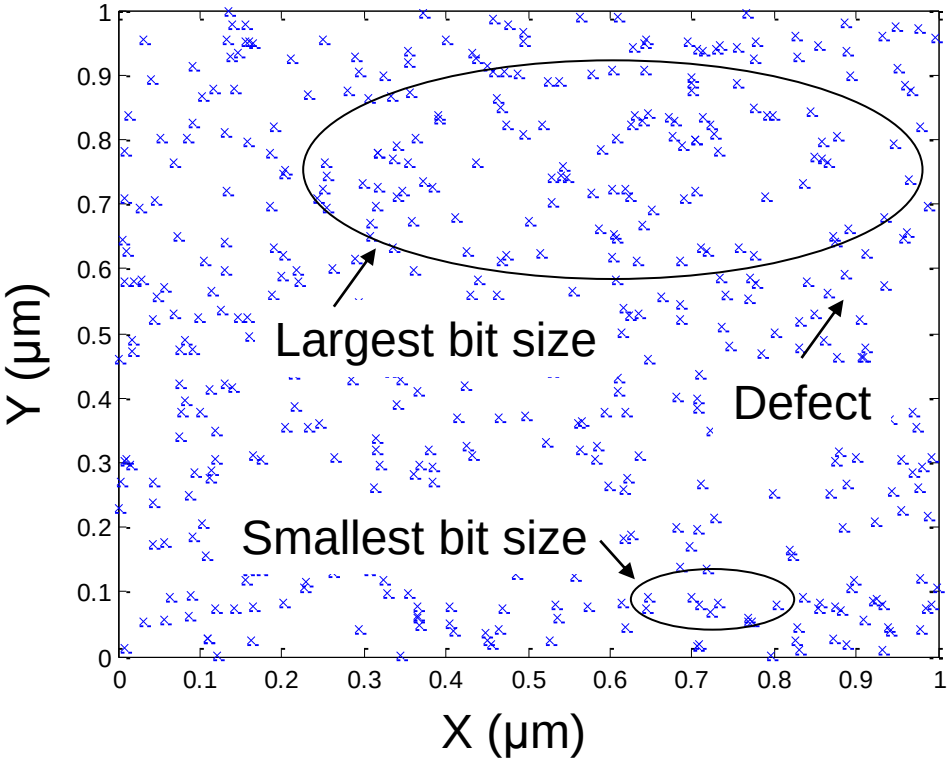
Tunneling AFM and Standard AFM of the same area



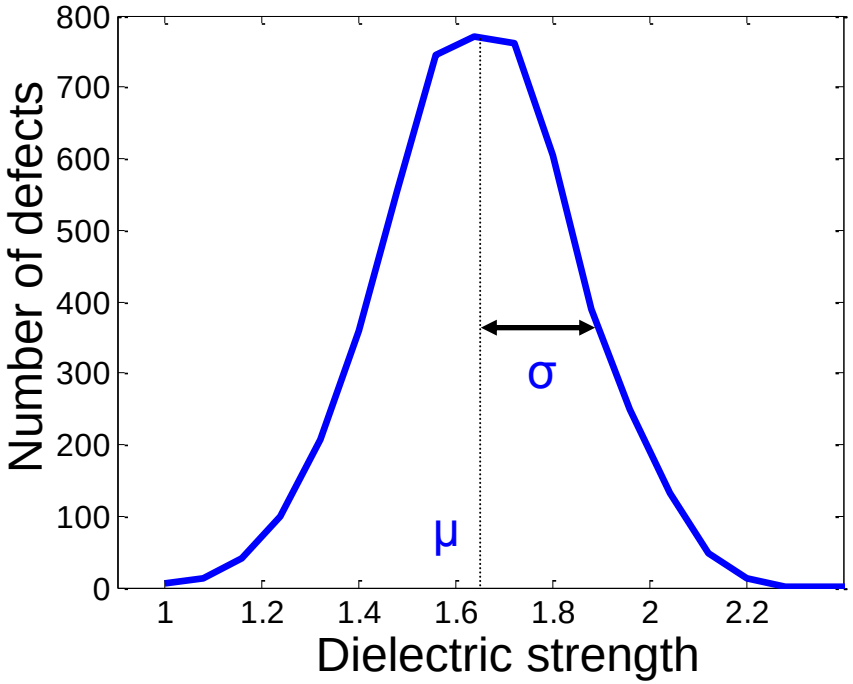
5µm × 5µm

Defect model for resistance and breakdown distributions

Random spatial distribution of defects

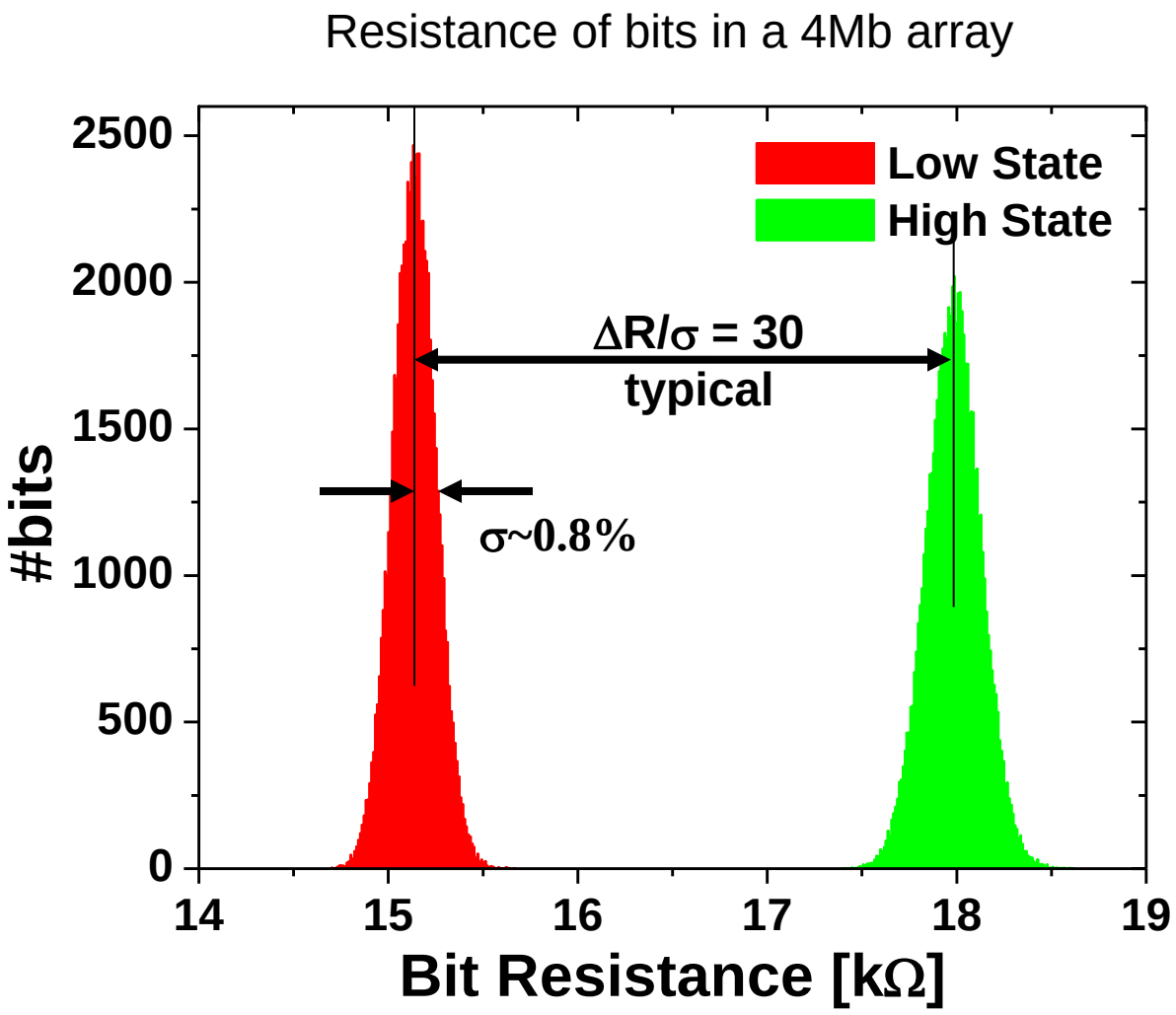


Each defect has associated dielectric strength drawn from normal distribution



- Breakdown mediated by weakest defect found in device

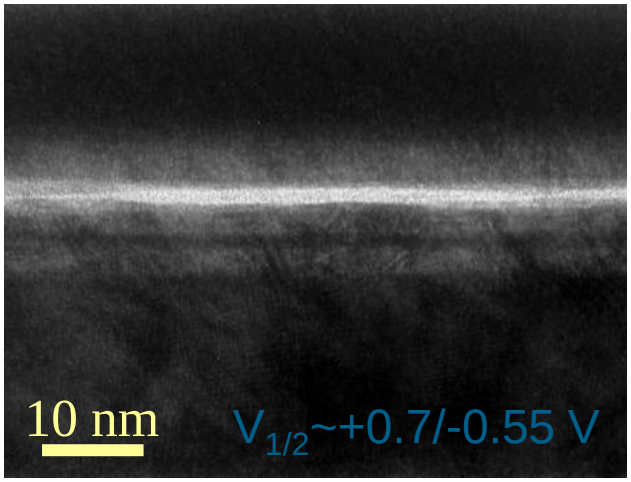
Read Distribution within an Array



Critical Factors:

1. Tunnel barrier quality
2. Pattern fidelity

Optimized for MRAM



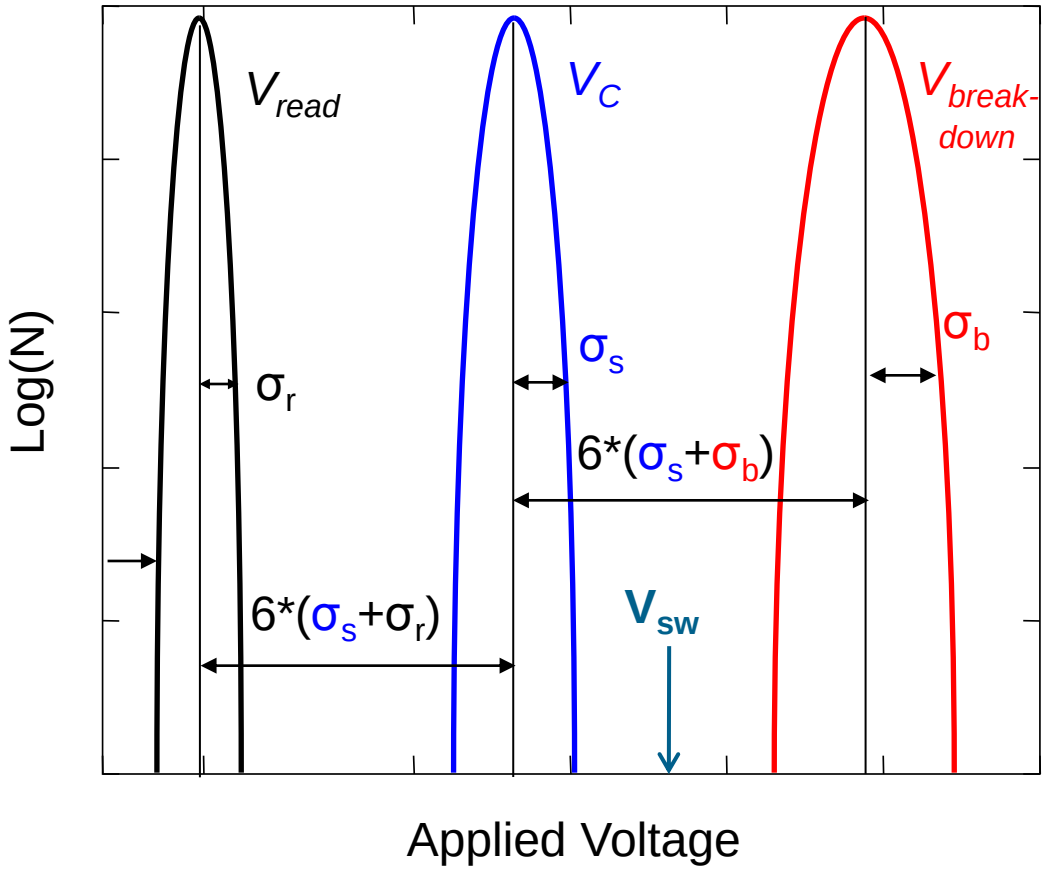
SPIN-TORQUE SWITCHING QUALITY

Single-bit data from probe of short-flow process wafers (not integrated with CMOS) with optimized structures and custom electronics for high-speed pulsing

Integrated memory array data from 16Mb test vehicle fabricated in 90nm CMOS logic process.

Distribution Considerations

Separation of distributions
Key criteria for working memory
MB memory ⇒ >12σ separation

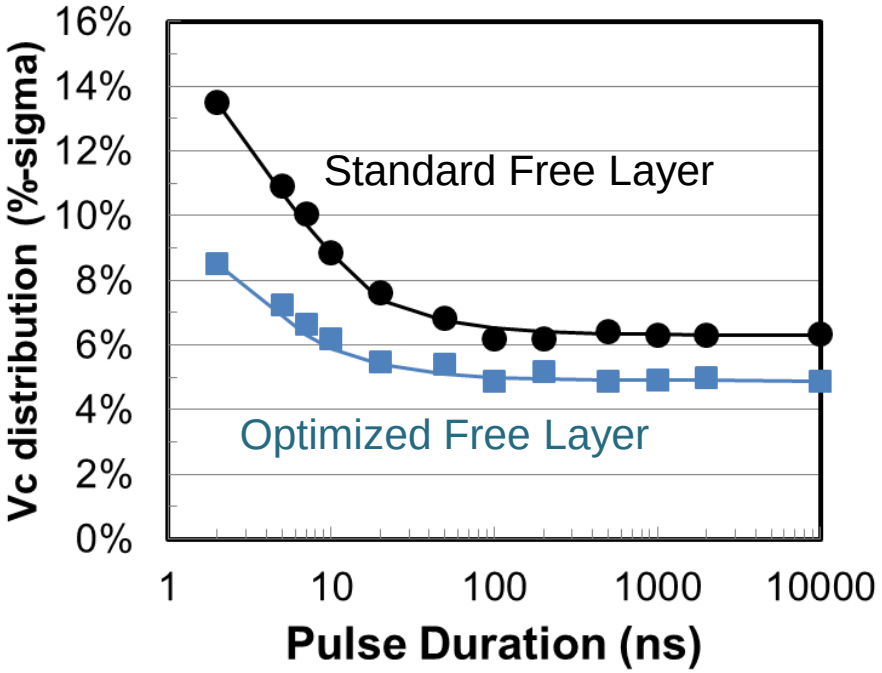


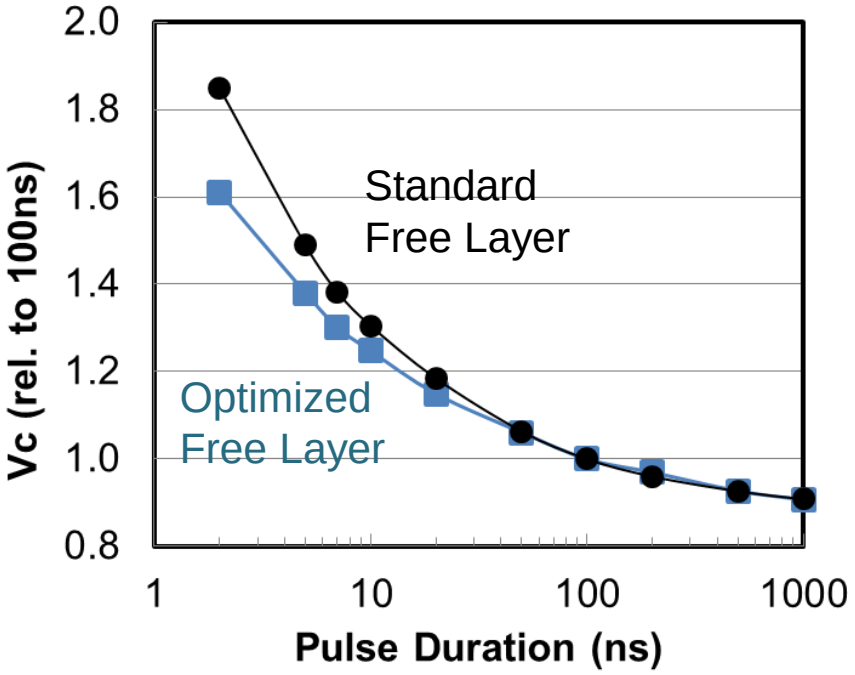
- **Separation of V_C & V_{bd}**
  - Reliable switching
  - Tunnel barrier reliability
- **Separation of V_{read} & V_C**
  - Avoid read-disturb errors
  - Bigger issue for smaller bits, lower I_C
- **Switching distribution width increased by:**
  - Shorter write pulses
  - Smaller bits
  - Extrinsic switching behavior

$$Separation = \frac{V_{bd} - V_C}{\sigma_{avg}}$$

Improved Switching in Arrays at High Speed

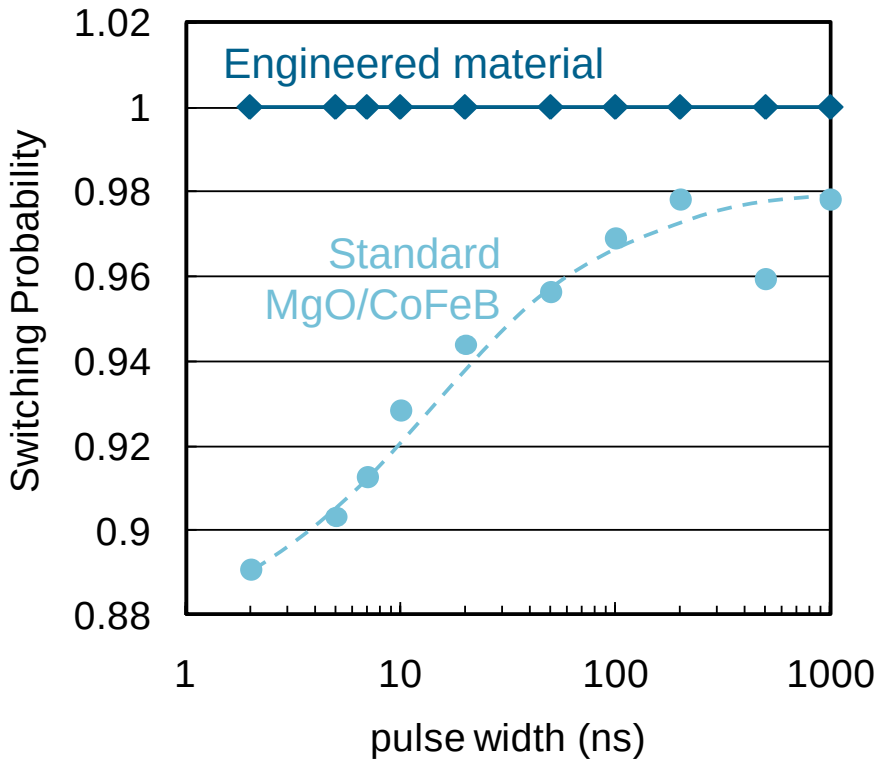
- **Optimized free layer material has better high-speed behavior**
  - Less increase in switching sigma for short pulses
    - Reduced single-bit sigma and less bit-to-bit variation
  - Less rise of Vc for short pulses
  - Fewer bits with anomalously high error rate





Data for integrated arrays of ~80nm bits

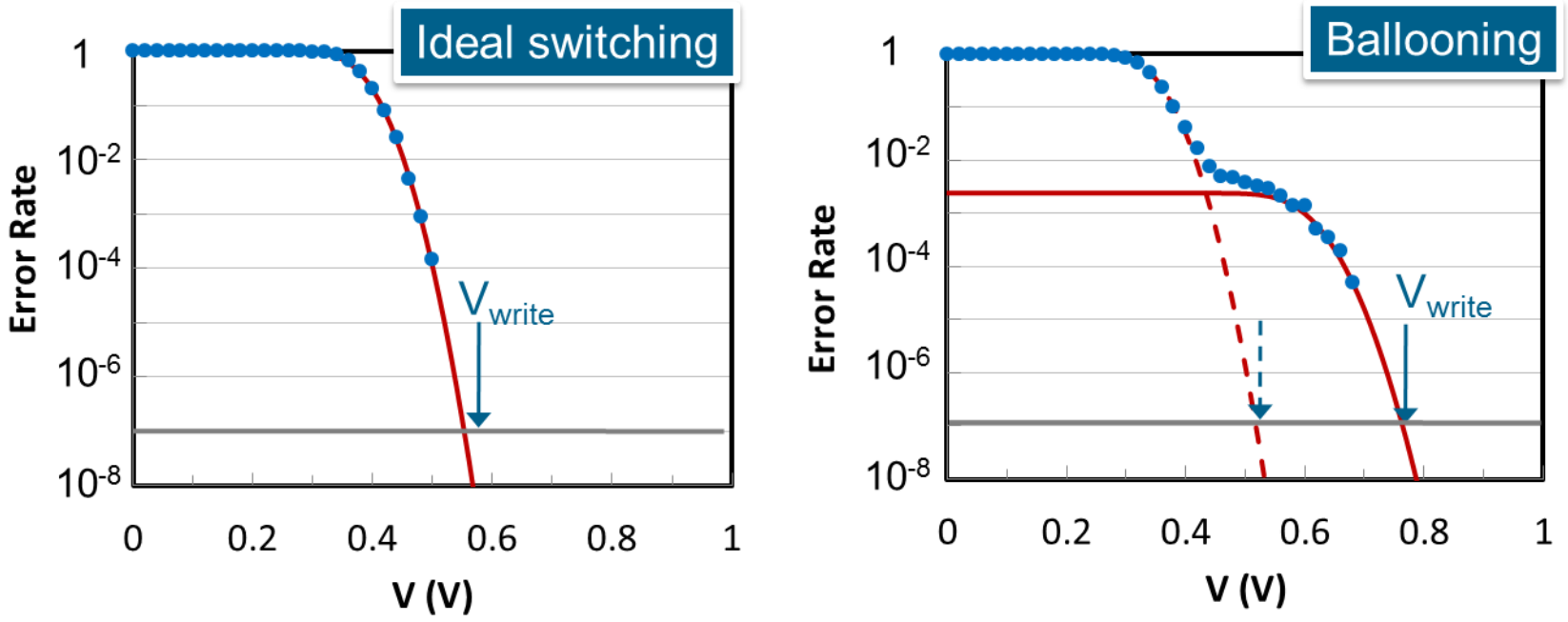
Reliable High-Speed Switching



- **Reliable high-speed switching with Everspin's engineered MTJ material**
  - **Reliable switching down to 2ns**
- **Standard CoFeB free layers have degraded switching at higher speed (shorter pulses)**
  - **Extrinsic bits cause trouble even for high applied bias.**

Switching Distribution Anomaly

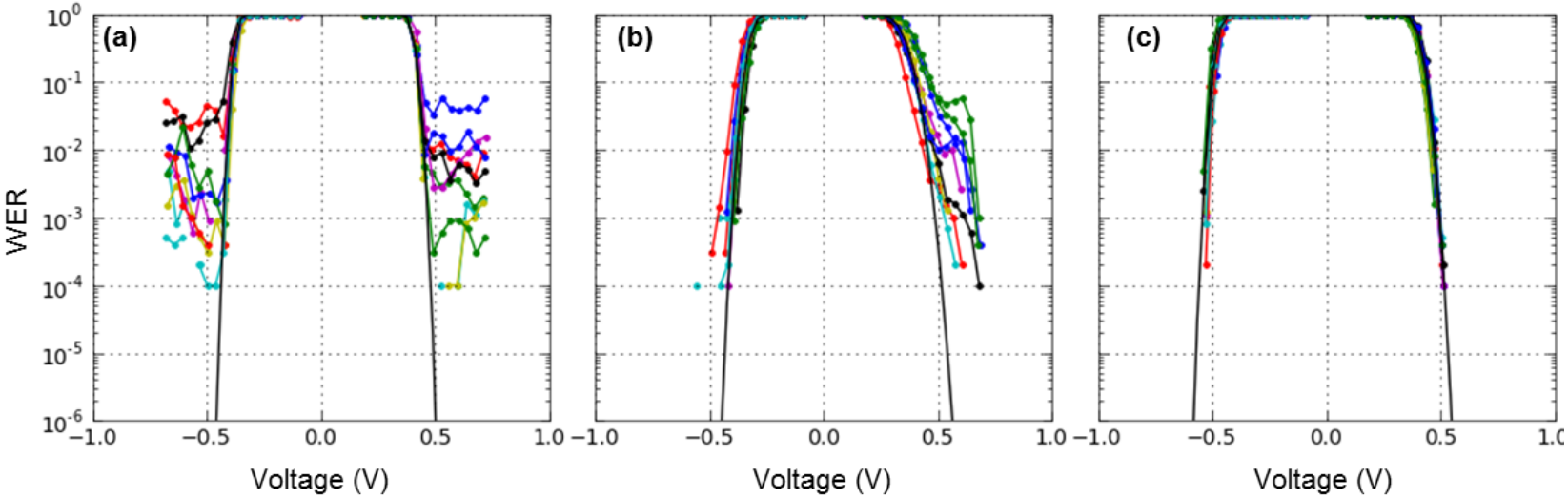
- **Some bits have non-Gaussian switching distributions**
  - 'Ballooning' effect results in higher write voltage requirement
  - Defect related. Caused by intermediate metastable magnetic state
    - Worse at high speed, not all bits exhibit this behavior



Single-bit switching distribution for 20,000 write cycles
Pulse width = 25ns

Continued improvements in switching quality

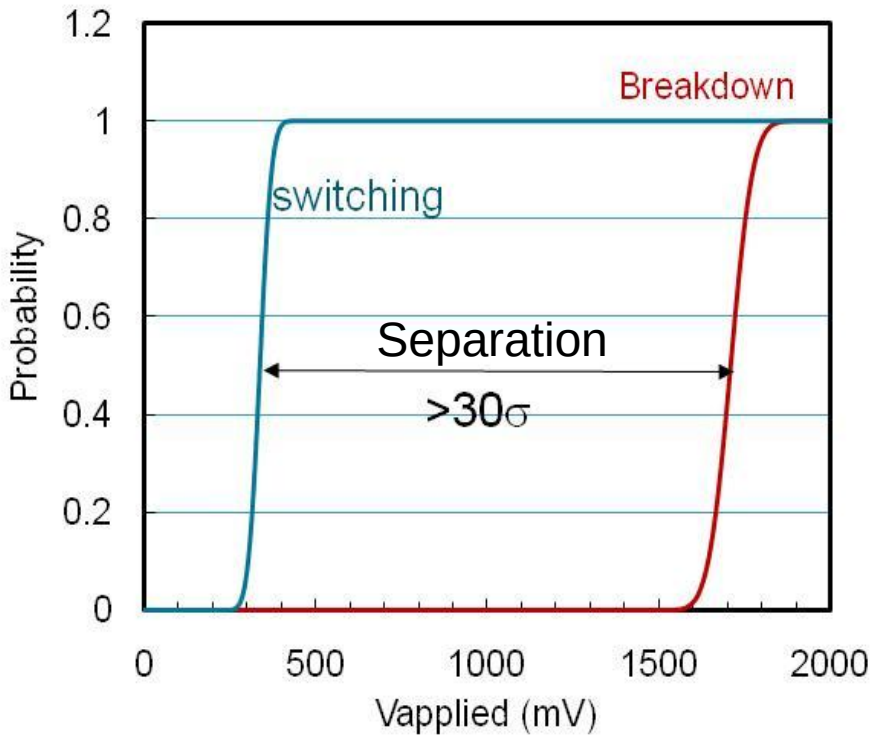
- **Optimized free layer improves both single-bit switching quality and bit-to-bit variation**



Write Error Rate (WER) out of 10,000 attempts for 9 bits, ~ 85nm x 240 nm , with write pulses of 25ns duration applied P-to-AP (V<0) and AP-to-P (V>0). The black line is a fit of the experimental data assuming a Gaussian distribution of WER.

Putting it all together

- **Demonstrated large separation of switching and breakdown in16 kb arrays integrated with CMOS**



- **Large separation >30σ**
- **Key figure of merit for:**
  - functionality
  - manufacturability
  - reliability

85 nm wide bits

Outline

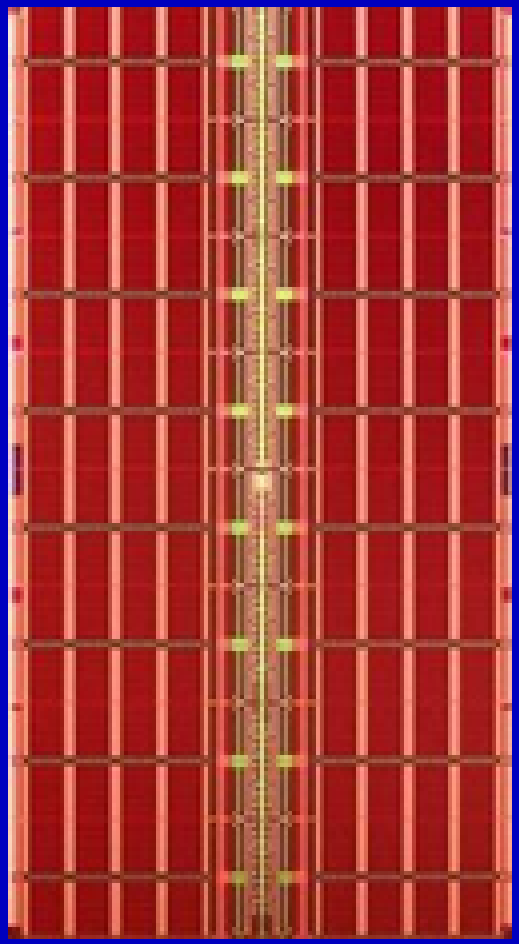
- MRAM overview
- Field-switched MRAM: “Classical Spintronics”
- Spin-torque MRAM: Spin-Torque-Transfer Spintronics
- Critical device properties and effect of materials
- **Status: Fully-functional 64Mb, DDR3 ST-MRAM**
- Summary

90nm DDR3 ST-MRAM Product

- 90nm Bulk Standard Process CMOS
- 4-Layer Metal + Al RDL

- 1.5V DDR3-1600, Ball Configuration
- Standard CAS Latency specs

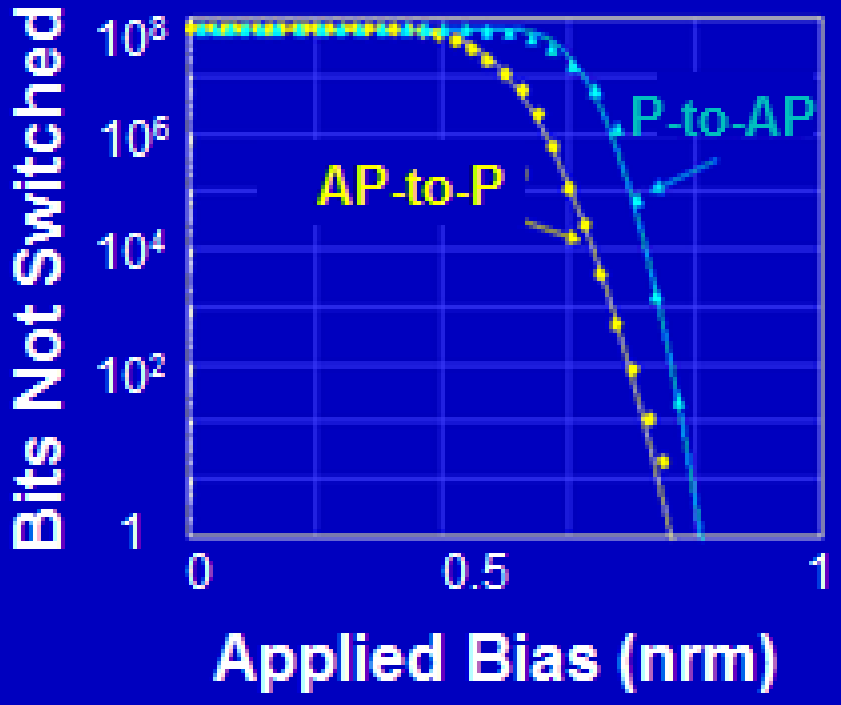
- Standard 8 bank architecture
- x4, x8, or x16 I/O configuration



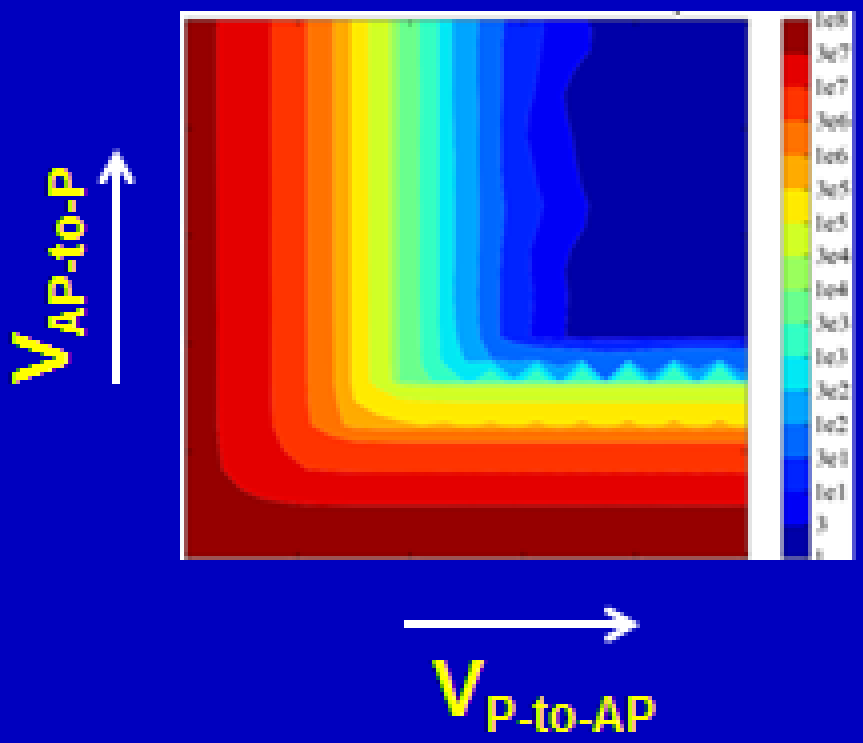
Switching in the 64Mb ST-MRAM

- **Normal distribution of switching voltage**

64Mb Switching Distributions

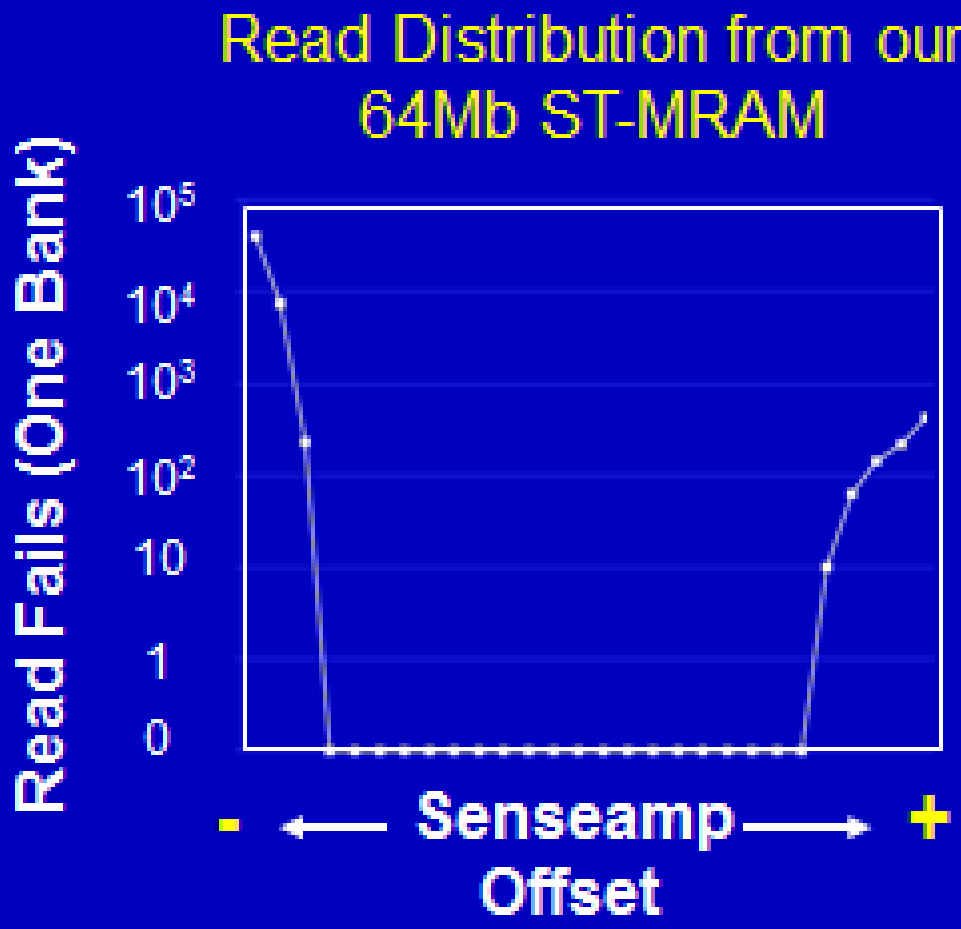


Operating Region for 1M March 6N Tests



Reading the 64Mb ST-MRAM

- Good read signal window – margin for speed



Conclusions

- **Toggle MRAM is a highly reliable, high-performance, nonvolatile memory, with unlimited endurance**
  - Product densities ranges from 256kb-16Mb
- **Spin-Torque MRAM technology is advancing to enable higher densities and lower power**
- **Continued developments and innovation in nano-magnetic switching provide a strong R&D pipeline for scaling and performance improvement.**
- **Demonstrated a fully-functional 64Mb DDR3 ST-MRAM and delivered working samples to customers**
  - Read and write with no errors
  - Gaussian switching distributions to ppm level
  - Arrays with >30-sigma separation of Vc and Vbd